AN2479
Application note

STA333ML demo board application note

Introduction

The purpose in this document is:

- to describe how to connect the STA333ML demo board,
- how to evaluate the demo board performance with electrical curve data,
- how to avoid critical board and layout issues.

Application note can be configured to the 2.0 channels only. Both of the 2 channels are in BTL mode. Each channel can deliver 20 W @ THD = 10% when Vcc = 18V and 8 load. It is a total solution for the digital audio power amplifier in a TV application.

All the test items and graph data in this document are measured by audio precision equipment. The test data shown in this document contains, for example, output power versus Vcc, frequency response, THD+N versus frequency, THD+N versus output power, FFT.

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1 Test condition and connection of demo board

1.1 Test condition

1.1.1 Jumper, power supply, signal and interface setting

1. JP1: format selection. 0[(a)] = I^2S, 1[(a.)] = left justified.
2. JP2: oversampling selection. 0 = 256 Fs, 1 = 384 Fs.
3. JP3: gain selection. 0 = 0 dB, 1 = +24 dB.
4. +3.3 V selection. Outer side = external +3.3 V, inner side = internal +3.3 V
5. Connect + voltage of 12 V DC power supply to +Vcc pin and negative to GND.
6. Connect + voltage of 3.3 V DC power supply to +3.3 V pin and negative to GND. If the +3.3 V selection is set to the inner side, do not connect this wire.
7. Connect GUI AP interface board to the J3 connector of STA333ML demo board.
8. Connect the S/PDIF signal cable to the RCA jack on the interface board, The input coming from the signal source such as Audio precision or DVD player.
9. The voltage range of the DC power supply for Vcc is from 5 V to 18 V.

1.1.2 Output configuration

STA333ML demo board can be configured to 2.0 channels and do not require software control. It is not necessary to connect the AP interface to the PC. When the power supply, signal, interface and output have been setup, push the RESET button which allows the STA333ML demo board to function.

1.2 Equipment requirement

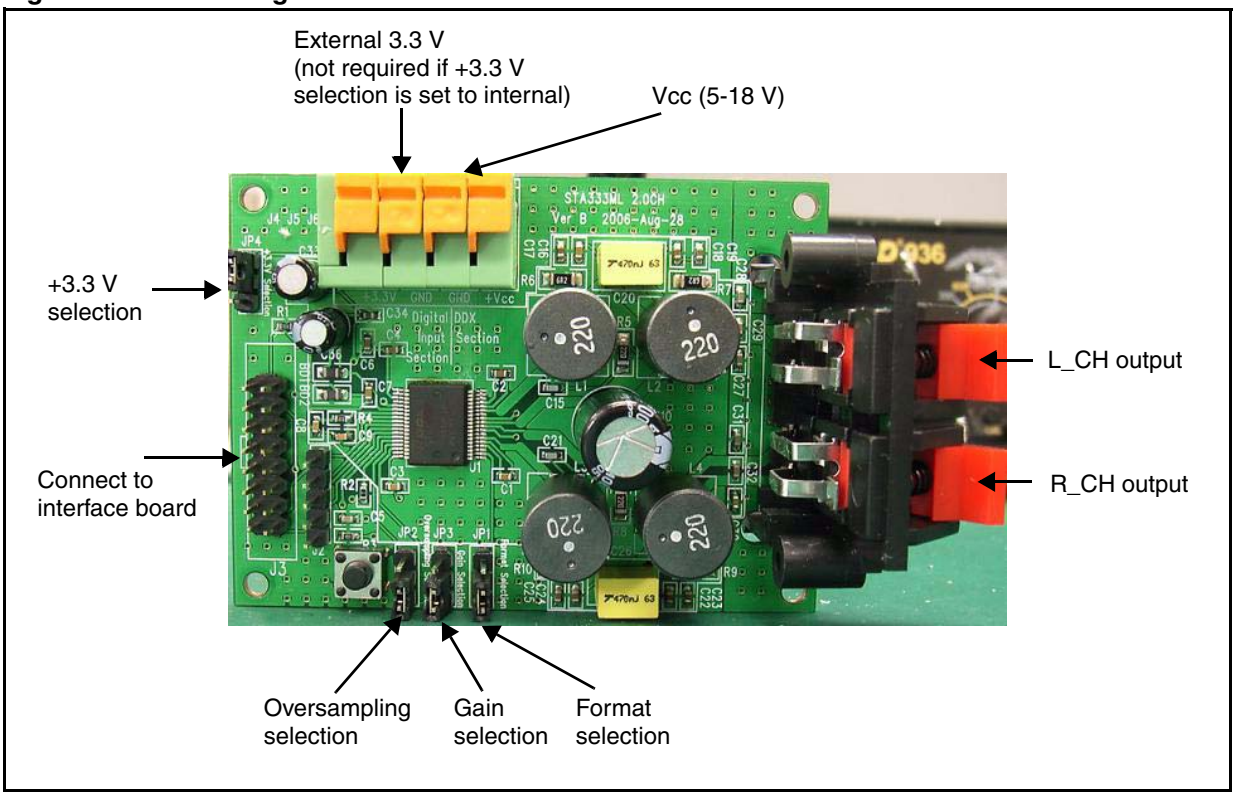
- Audio Precision (System 2700) by AP Co., USA)
- DC power supply (With 5V to 18V)
- Digital oscilloscope (TDS3034B) by Tektronix
- PC

a. 0: connect to outer side, 1: connect to inner side.

1.3 Connection method

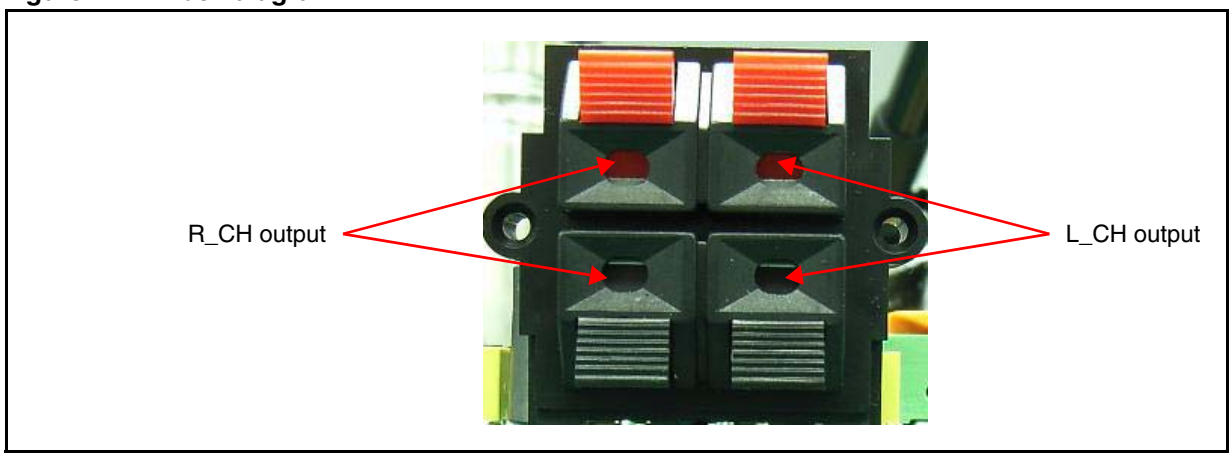
Top view of demo board.

Figure 1. Block diagram



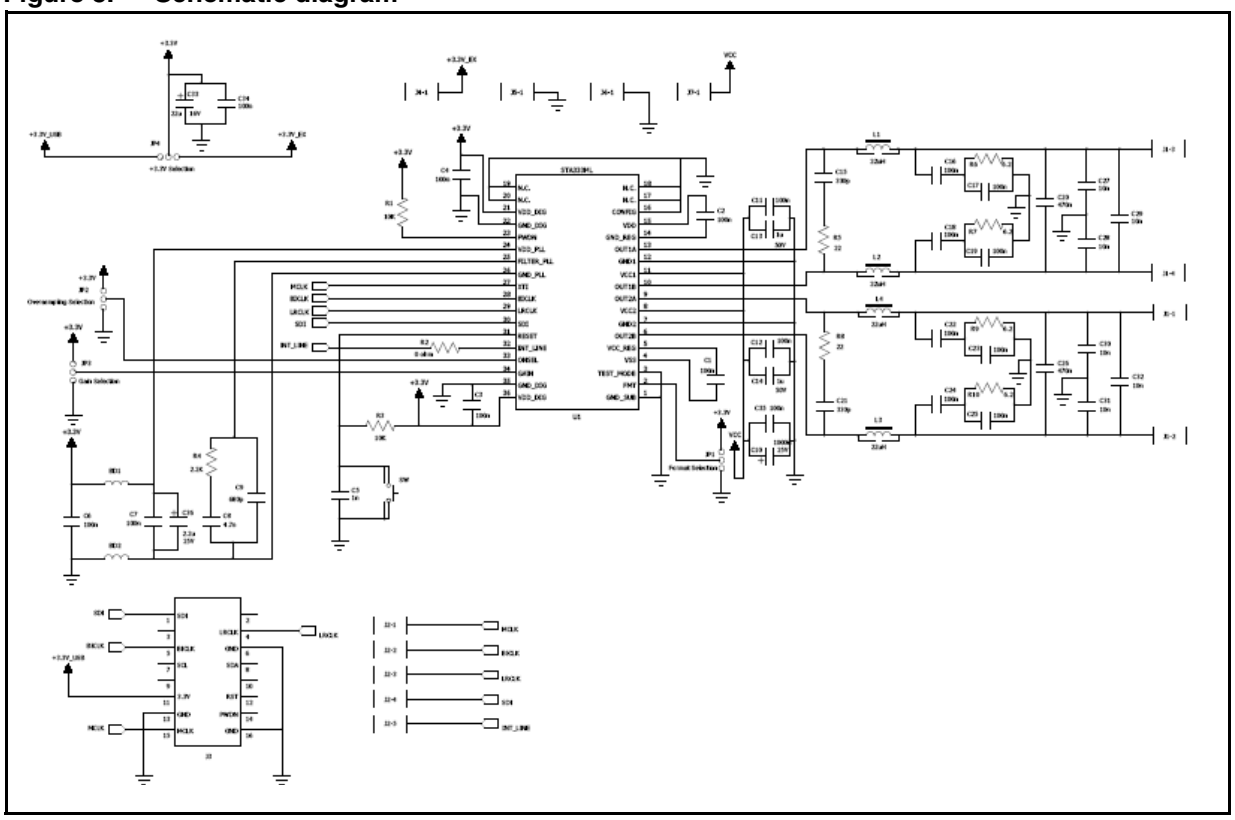
1.3.1 Speaker jack connection

Figure 2. Block diagram



1.3.2 Schematic

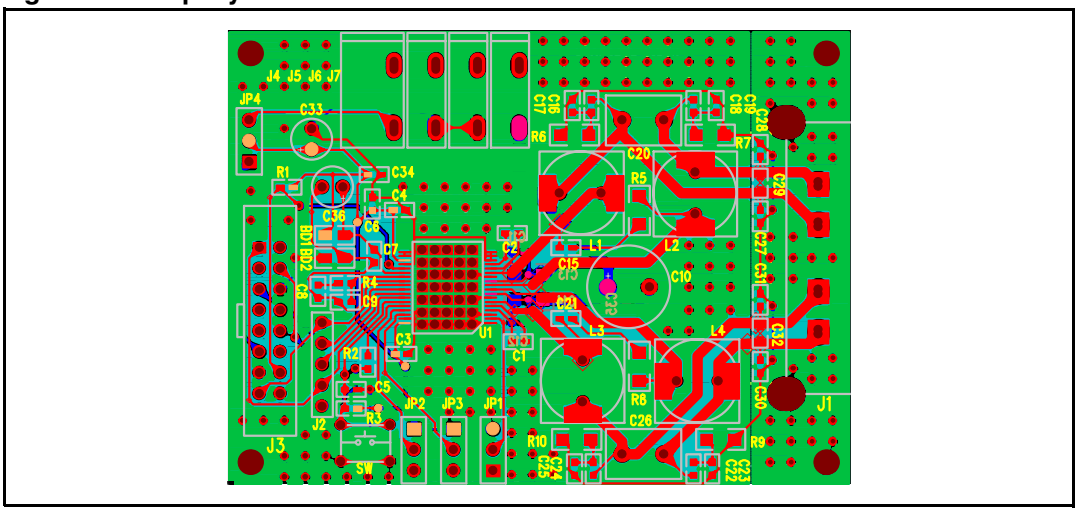
Figure 3. Schematic diagram



1.4 PCB Layout

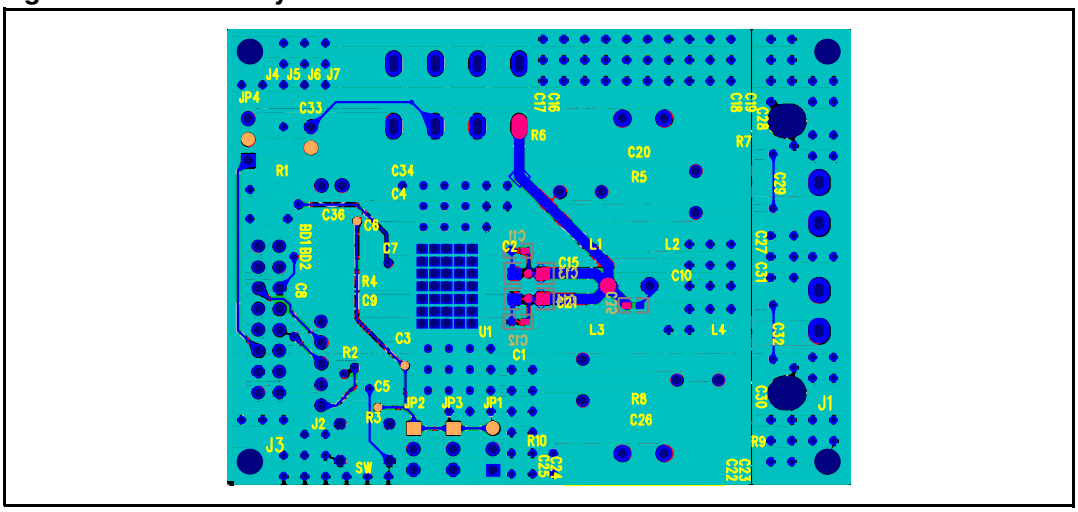
1.4.1 Top view of PCB layout

Figure 4. Top layout



1.4.2 Bottom view of PCB layout

Figure 5. Bottom layout



1.5 BOM list

Table 1. BOM

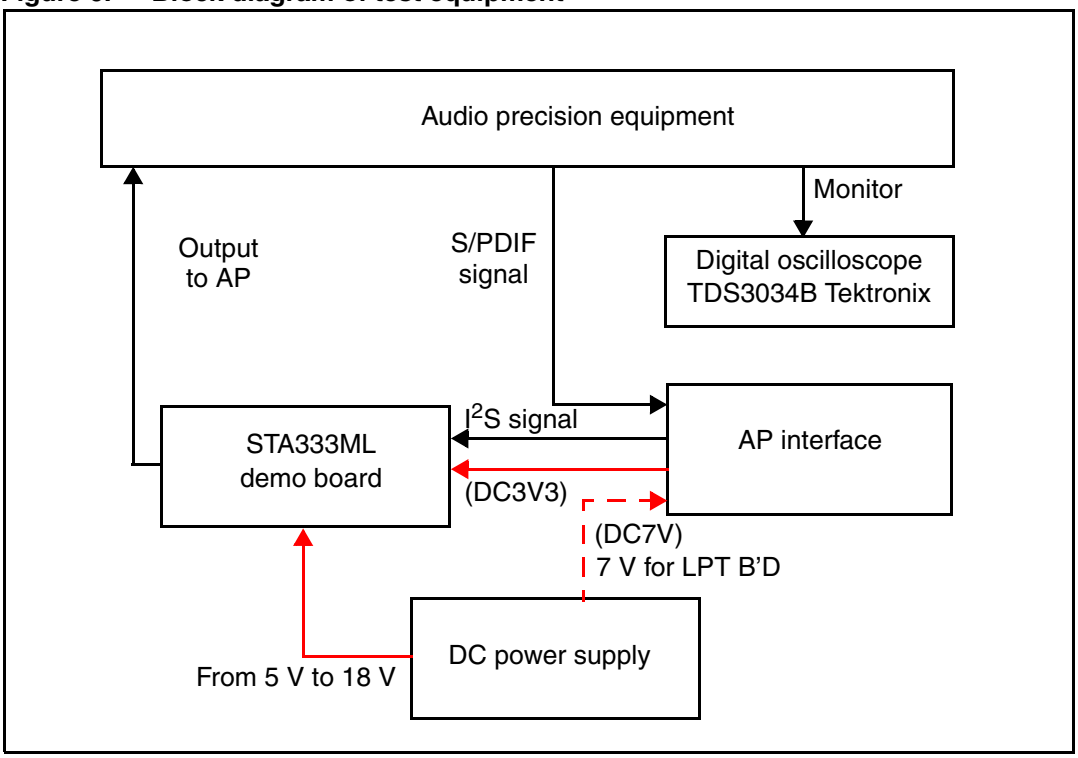
Item no.	Type	Package	Description	Qty	Reference code	Manufacturer
1	CCAP	CCAP0603	100 n, 50 V, +/- 10 %	18	C1, C2, C3, C4, C6, C7, C11, C12, C16, C17, C18, C19, C22, C23, C24, C25, C34, C35	Murata
2	CCAP	CCAP0603	1 n, 50 V, +/- 10 %	1	C5	Murata
3	CCAP	CCAP0603	4.7 n, 50 V, +/- 10 %	1	C8	Murata
4	CCAP	CCAP0603	680 p, 50 V, +/- 5 %	1	C9	Murata
5	CCAP	CCAP0603	330 p, 50 V, +/- 10 %	2	C15, C21	Murata
6	CCAP	CCAP0603	10 n, 50 V, +/- 10 %	6	C27, C28, C29, C30, C31, C32	Murata
7	CCAP	CCAP1206	1 µ, 50 V	2	C13, C14	Murata
8	ECAP	D = 10 mm	1000 µ, 25 V	1	C10	Rubycon
9	ECAP	D = 7 mm	22 µ, 16 V	1	C33	Rubycon
10	ECAP	D = 5 mm	2.2 µ, 25 V	1	C36	Rubycon
11	Chip bead	L0805	600 ohm @ 100 MHz	2	BD1, BD2	Murata
12	CRES	R0603	10 k +/- 5 %	2	R1, R3	Murata
13	CRES	R0603	0 ohm +/- 5 %	1	R2	Murata
14	CRES	R0603	2.2 k +/- 5 %	1	R4	Murata
15	CRES	R1206	22 ohm +/- 5 %	2	R5, R8	Murata
16	CRES	R1206	6.2 ohm +/- 5 %	4	R6, R7, R9, R10	Murata

Table 1. BOM

Item no.	Type	Package	Description	Qty	Reference code	Manufacturer
17	Test point	Through hole	1 x 5 2.54 mm pitch	1	J2	Any source
18	Connector	Through hole	2 x 8 2.54 pitch male connector	1	J3	Any source
19	Jumper	Through hole	1 x 3 2.54 mm pitch	4	JP1, JP2, JP3, JP4	Any source
20	IC	Through hole	STA333ML	1	U1	ST
21	CAP	Through hole	470 n	2	C20, C26	
22	Connector	Through hole	WP4-15	1	J1	Song Cheng
23	Connector	Through hole	FFKDS/H1-5.08	3	J5, J6, J7	Phoenix contact
24	Connector	Through hole	FFKDSA1/H1-7.62	1	J4	Phoenix contact
25	COIL	Through hole	22 µH	4	L1, L2, L3, L4	Kwang Sung
26	Tact switch	Through hole	6 x 6 Tact switch	1	SW	

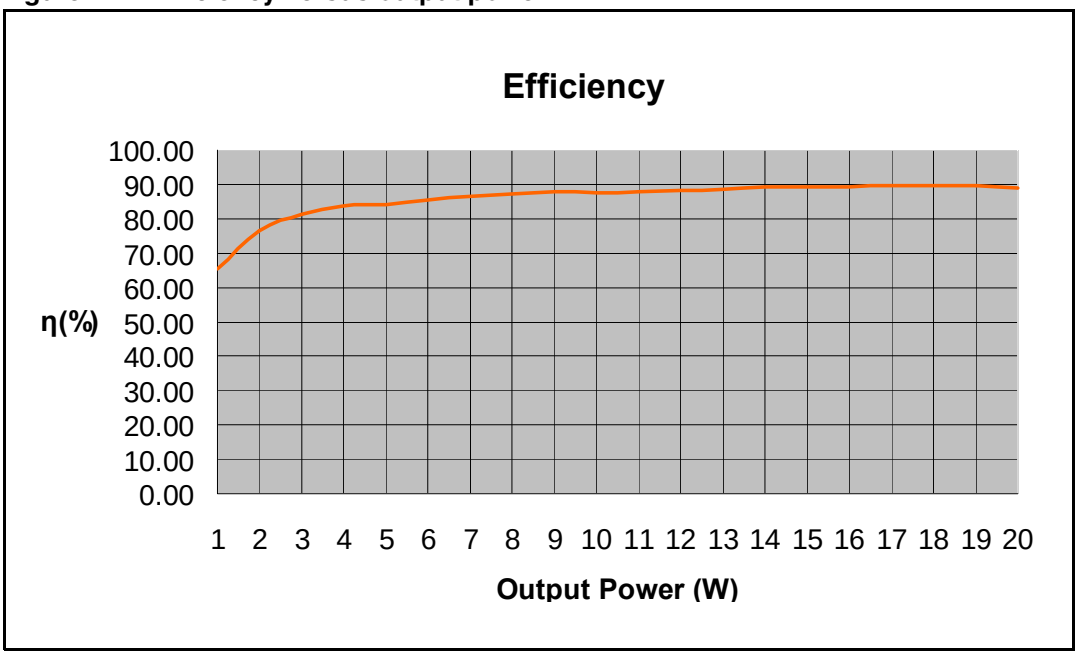
1.5.1 Test connection

Figure 6. Block diagram of test equipment



2 Test curve report

Figure 7. Efficiency versus output power



Condition: R LOAD =8 ohm; VCC=18 V

Figure 8. Output power versus Vcc

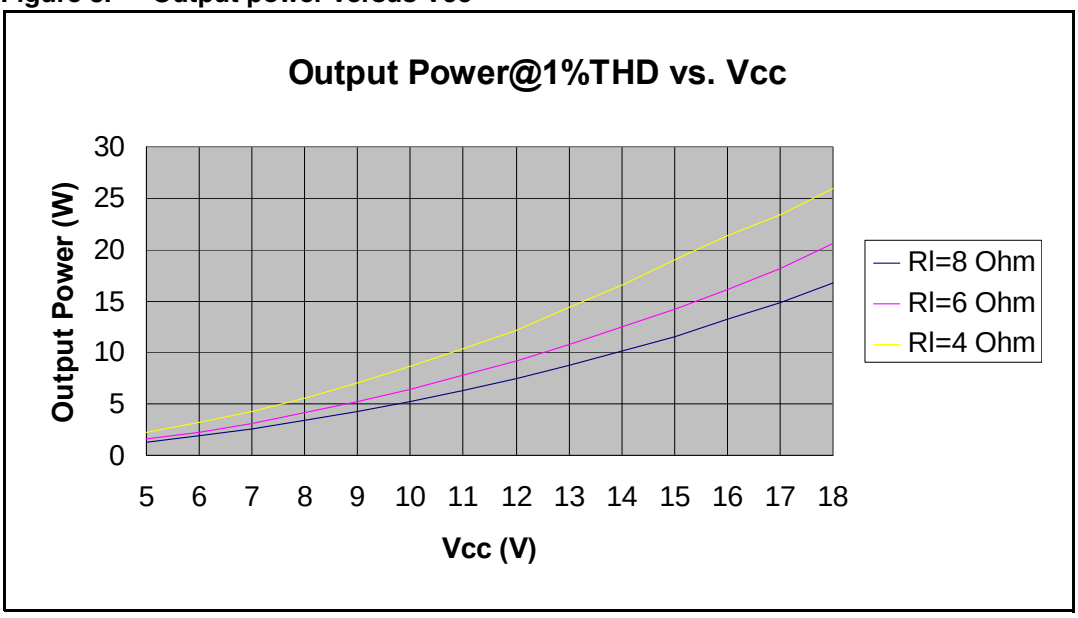
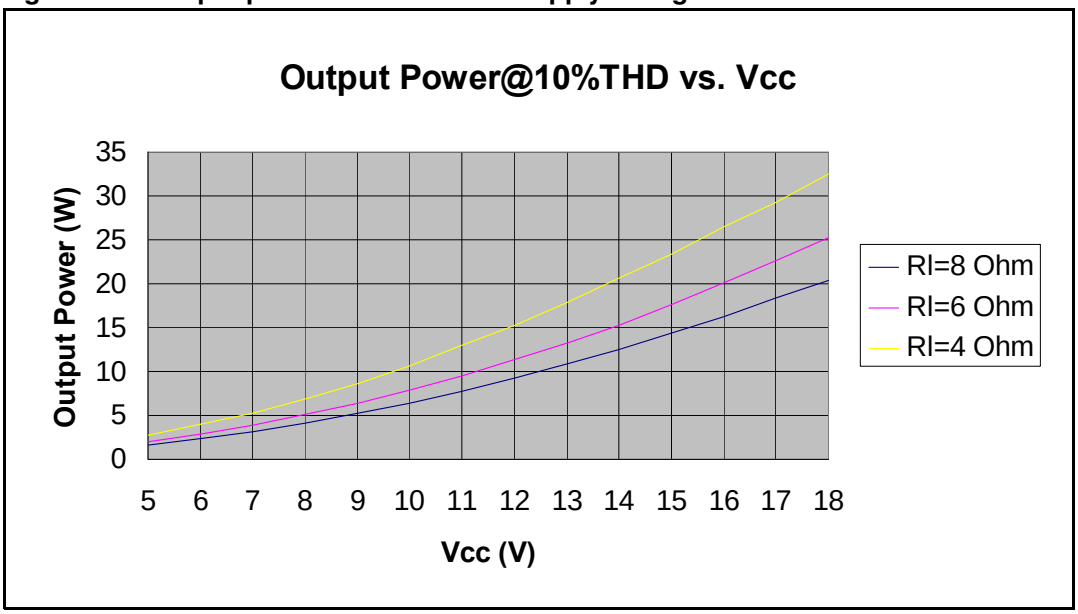


Figure 9. Output power@10% THD vs. supply voltage



2.1 Frequency Response

Figure 10. 18 V 4 ohm 0 dB: Pout = 1 W@ 1 KHz filter: L = 10 uH, C = 1 uF

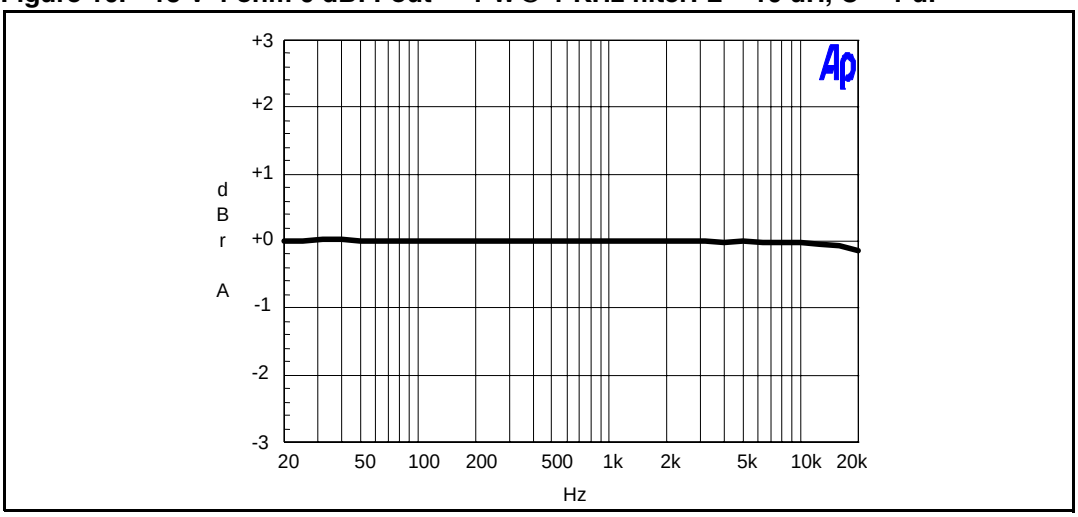


Figure 11. 18 V 6 Ohm 0 dB: Pout = 1 W @ 1 KHz filter: L = 15 uH, C = 680 nF

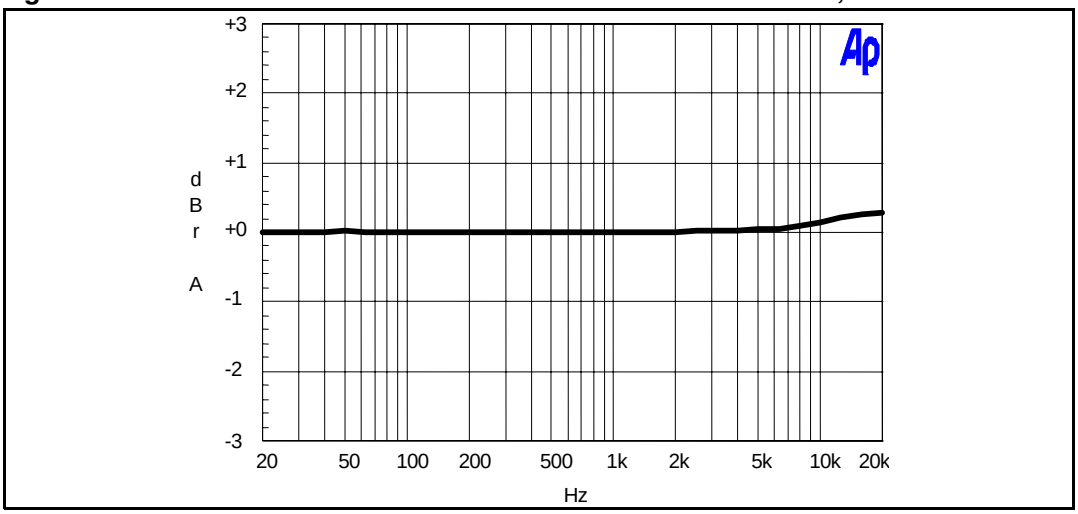


Figure 12. 18 V 8 Ohm 0 dB: Pout = 1 W @ 1 KHz filter: L = 22 uH, C = 470 nF

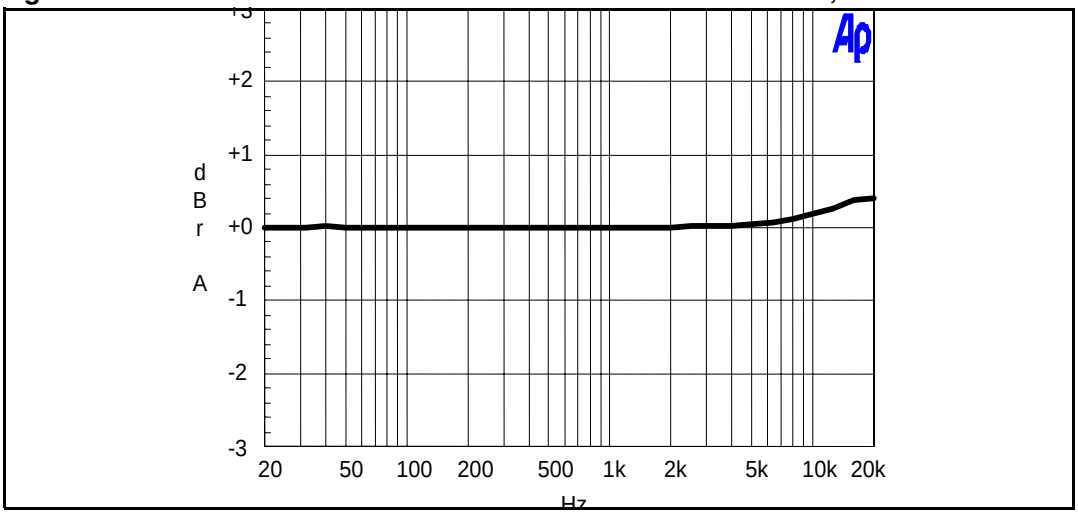
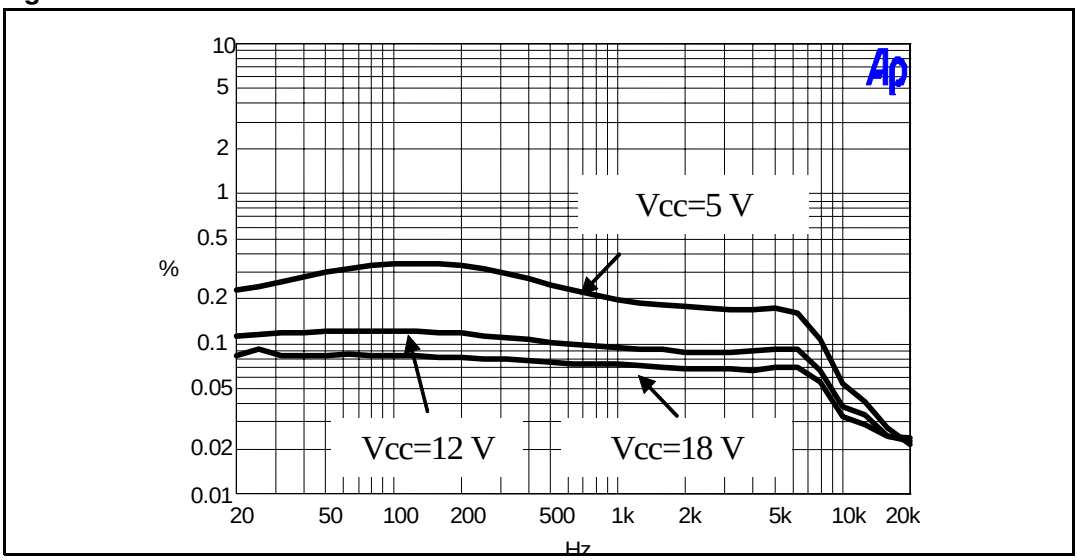


Figure 13. 6 Ohm Pout = 1 W



2.2 THD versus frequency

Figure 14. 4 Ohm Pout = 1 W

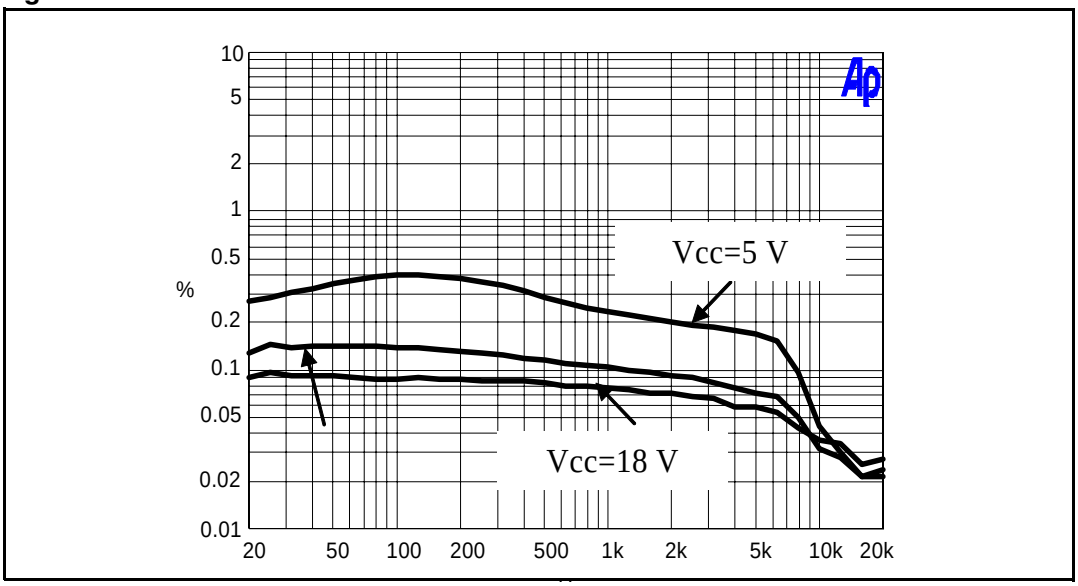
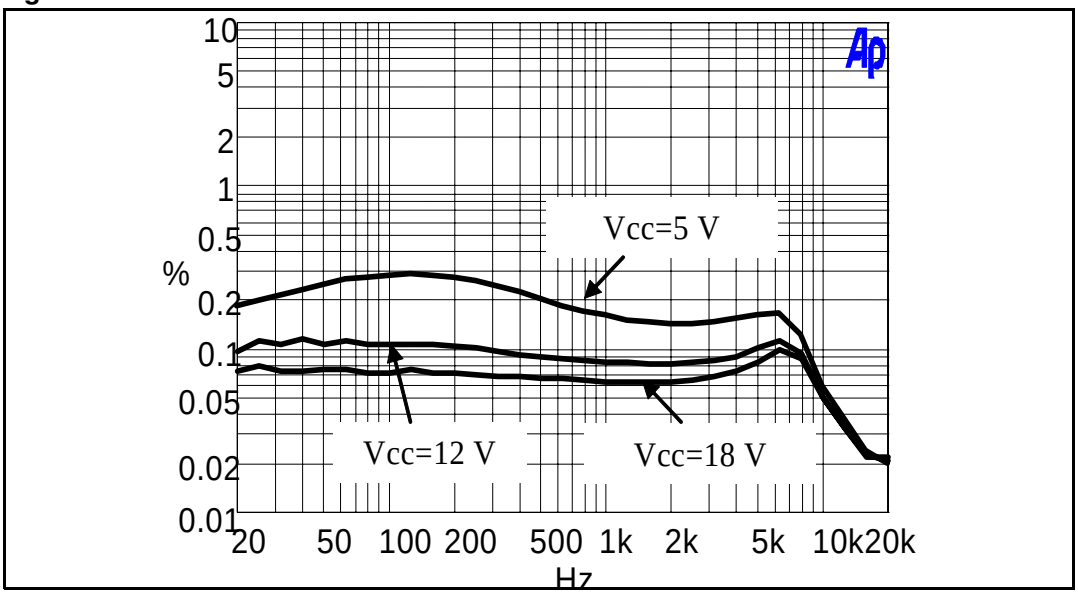


Figure 15. 8 Ohm Pout = 1 W



2.2.1 THD versus output power

Figure 16. 4 Ohm (1/2)

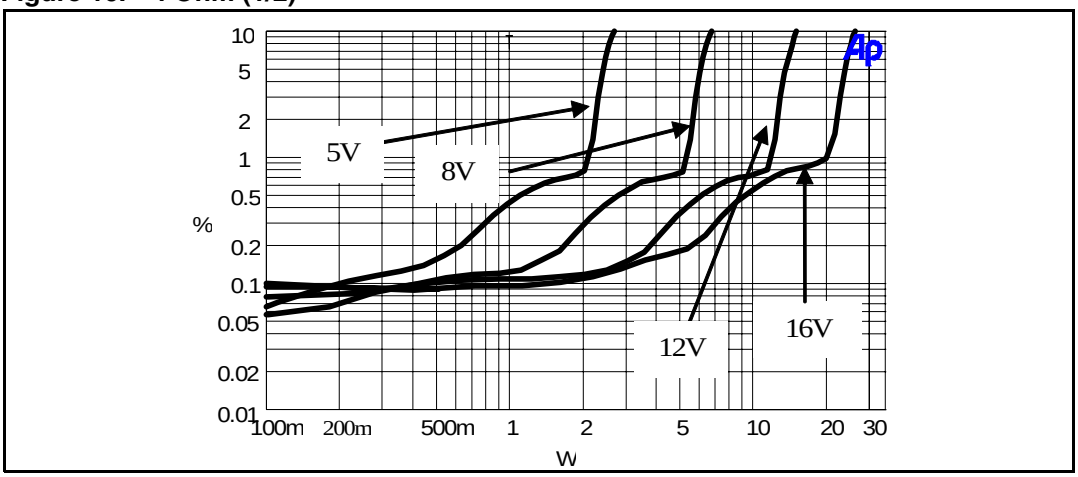


Figure 17. 4 Ohm (2/2)

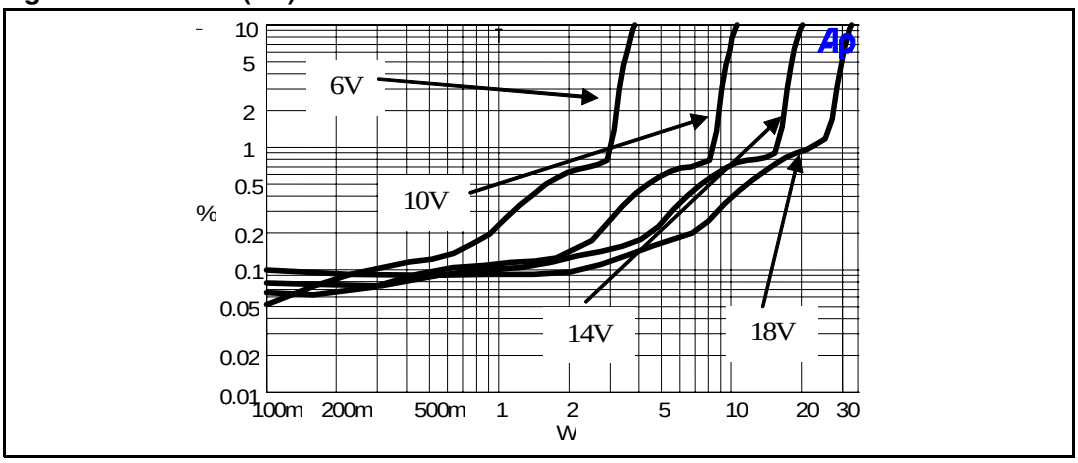


Figure 18. 6 Ohm (1/2)

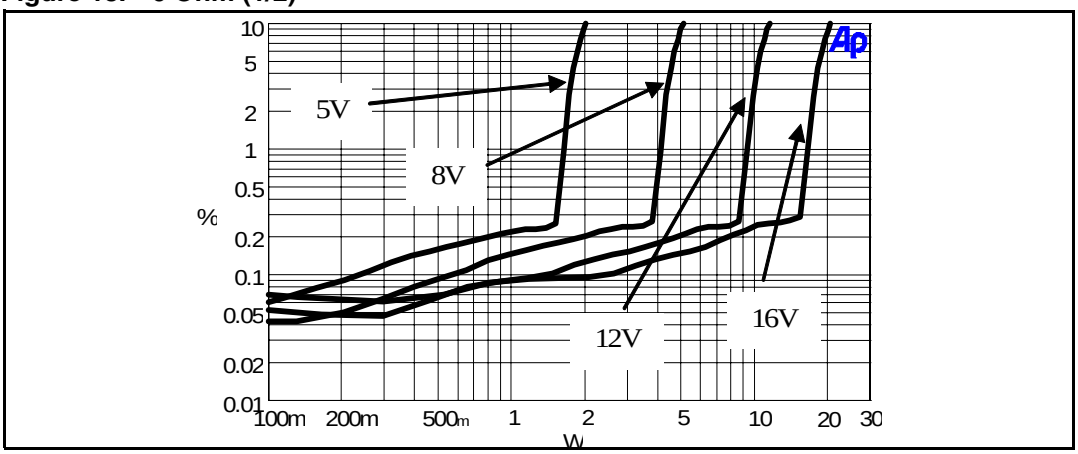


Figure 19. 6 Ohm (2/2)

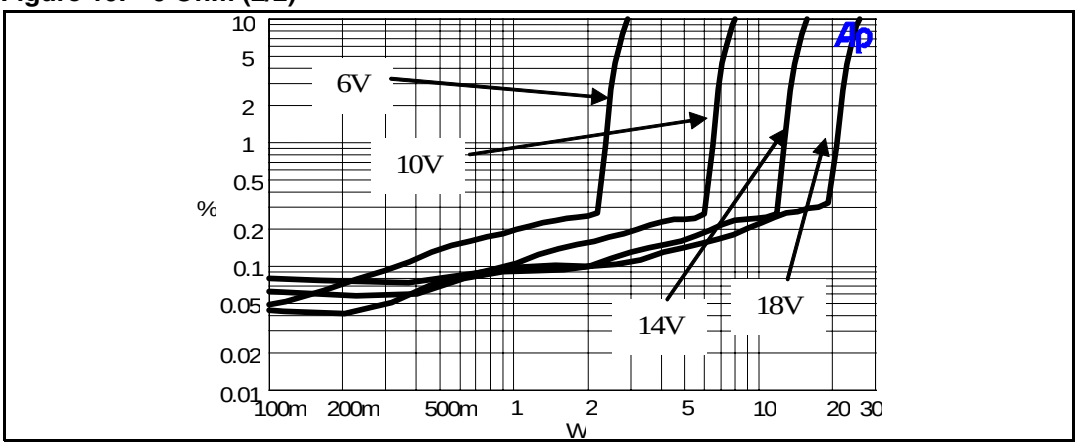


Figure 20. 8 Ohm (1/2)

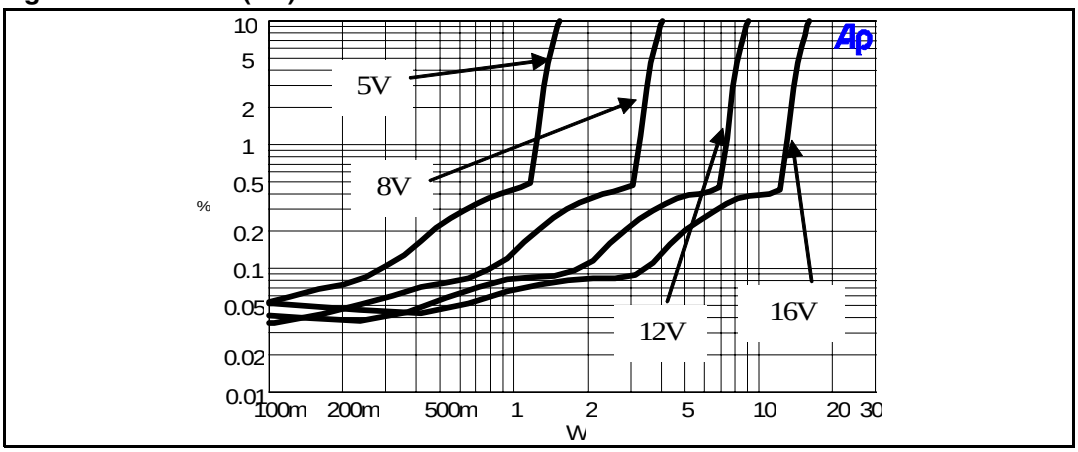
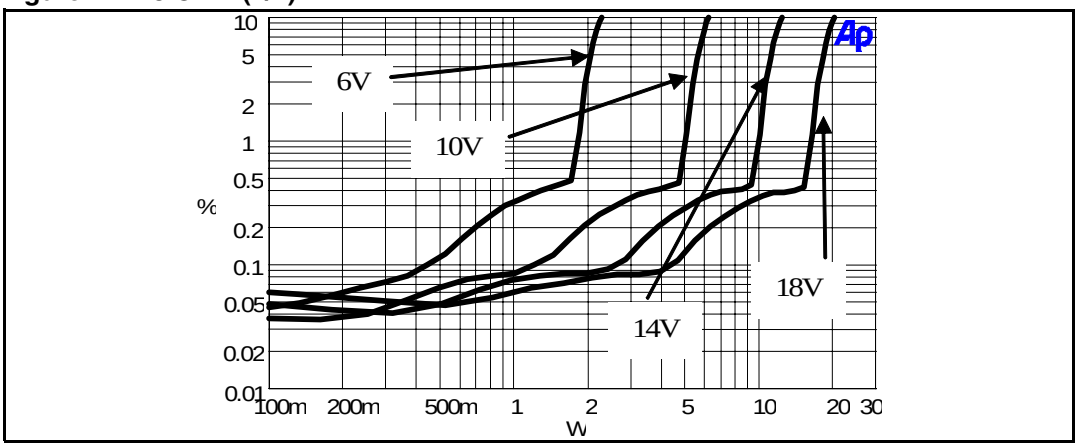


Figure 21. 8 Ohm (2/2)



2.3 FFT

Figure 22. 0 dBFS@ 1 KHz 5 V 4 ohm

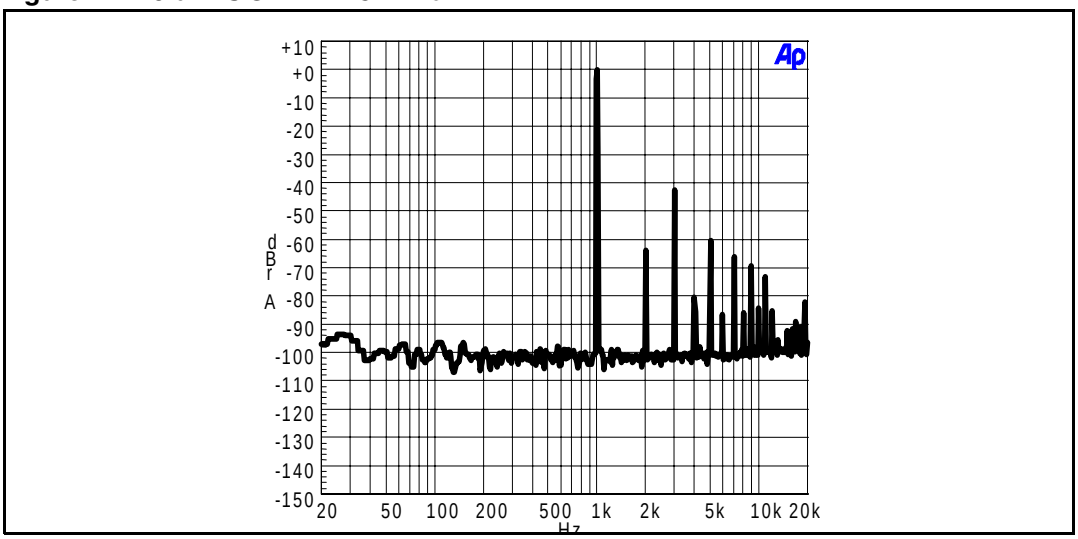


Figure 23. -60 dBFS@ 1 KHz 5 V 4 ohm

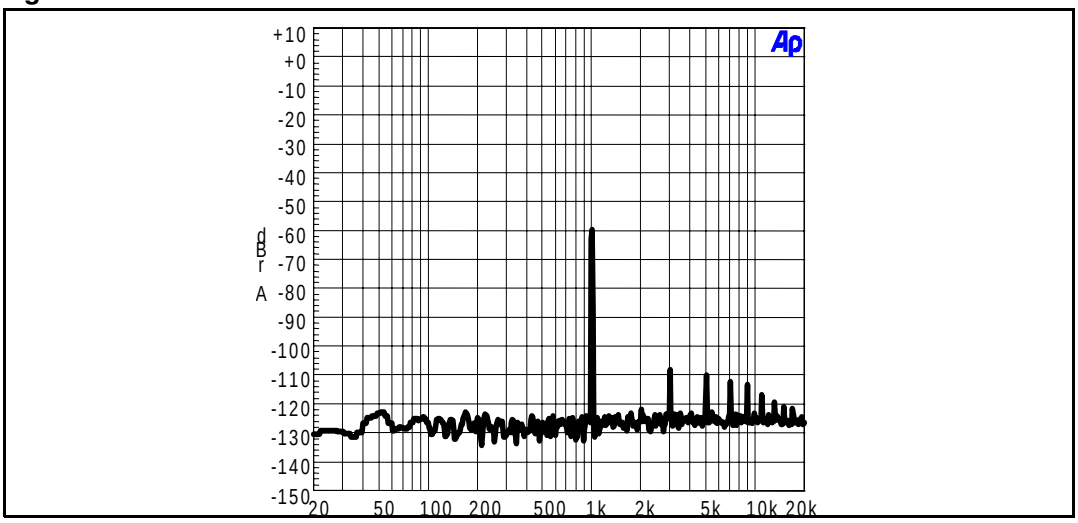


Figure 24. 0 dBFS@ 1 KHz 5 V 6 ohm

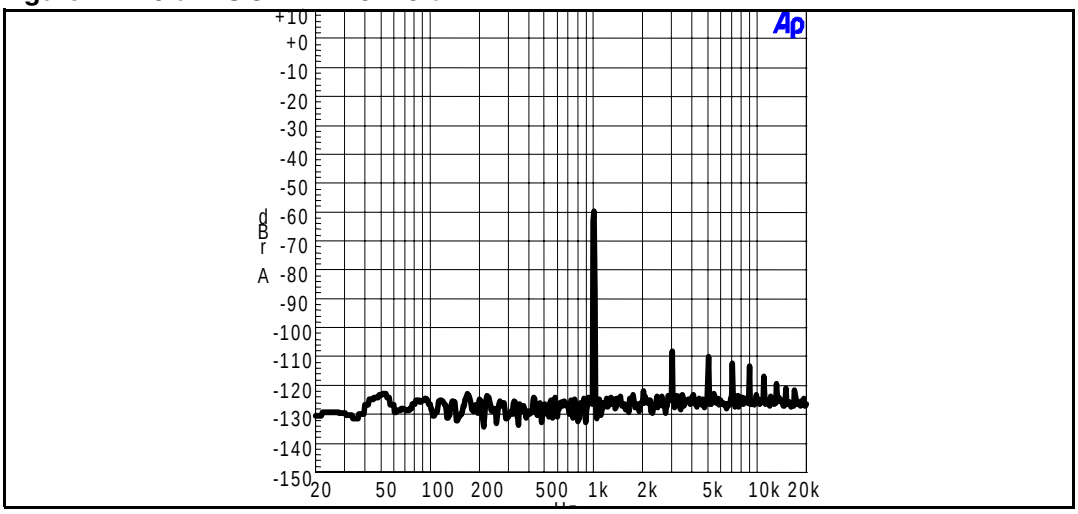


Figure 25. -60 dBFS@ 1 KHz 5 V 6 ohm

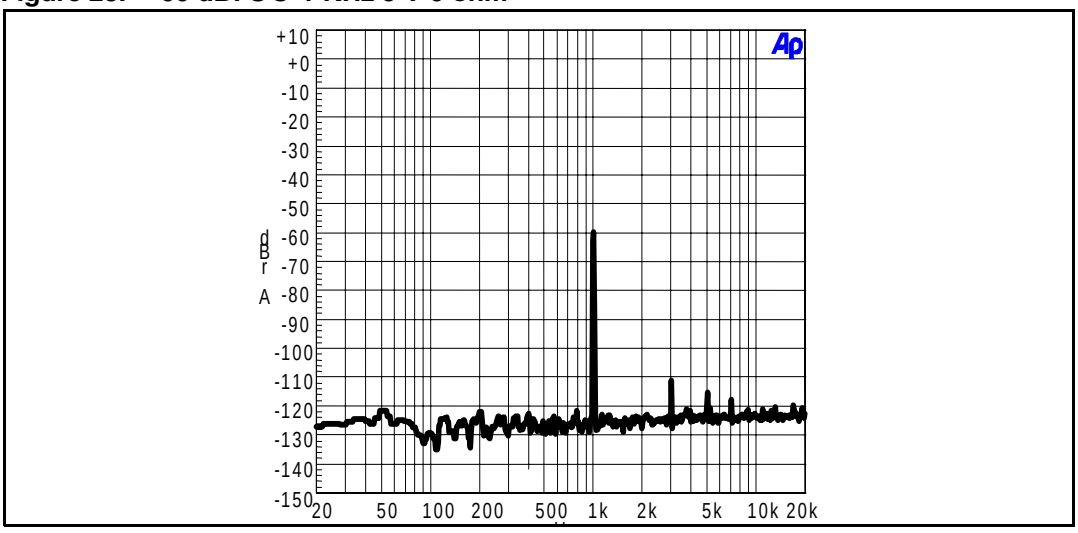


Figure 26. 0 dBFS@ 1 KHz 5 V 8 ohm

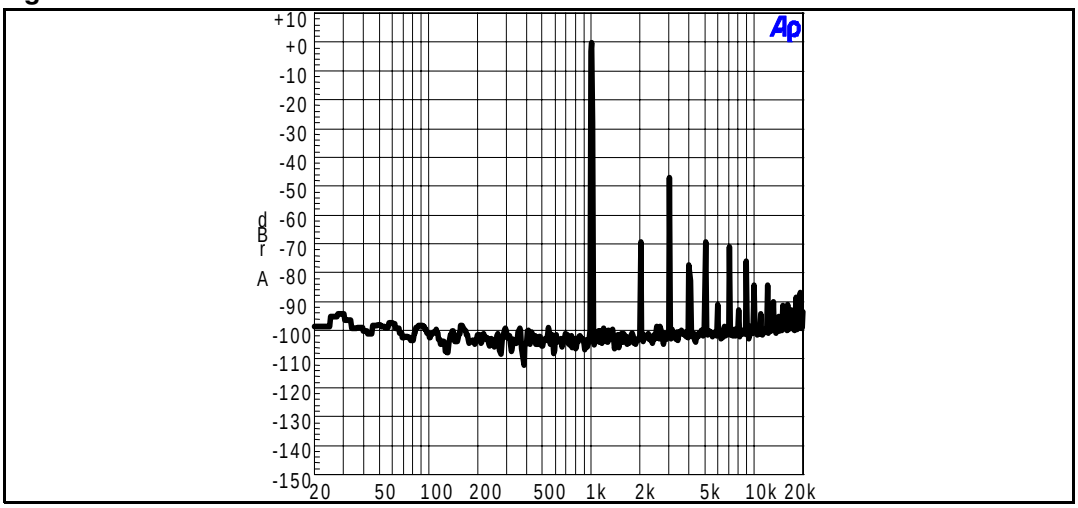


Figure 27. -60 dBFS@ 1 KHz 5 V 8 ohm

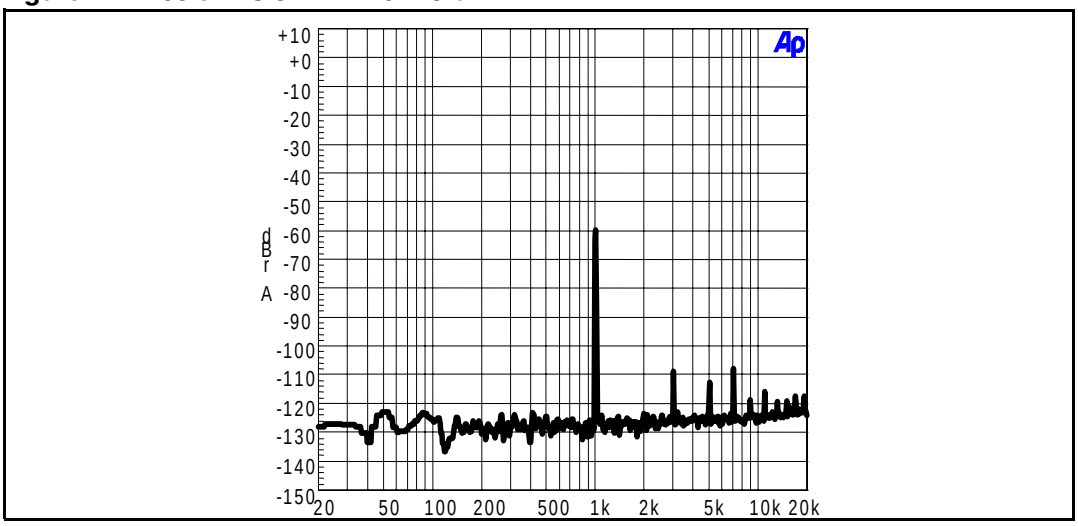


Figure 28. 0 dBFS@ 1 KHz 12 V 4 ohm

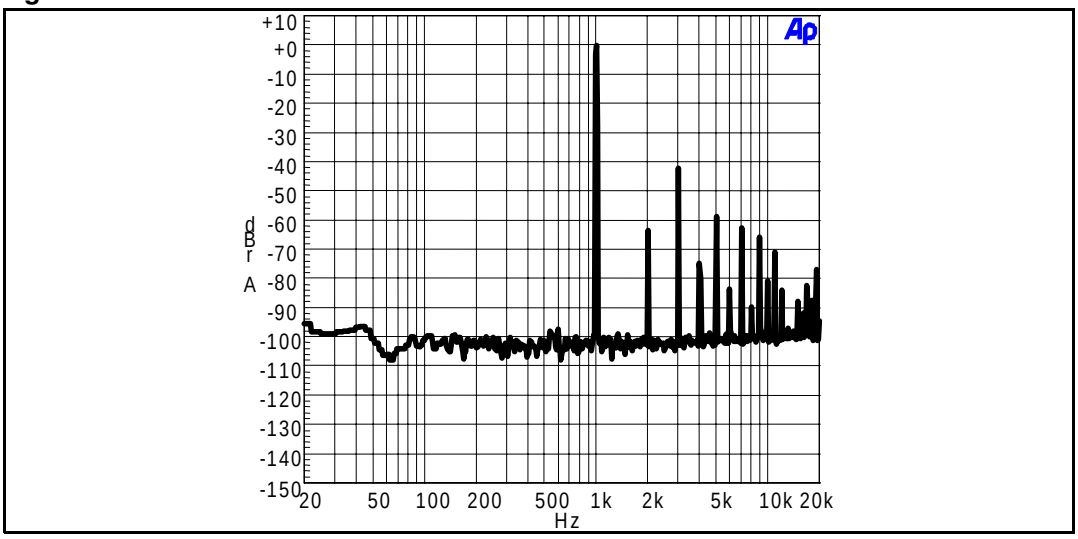


Figure 29. -60 dBFS@ 1 KHz 12 V 4 ohm

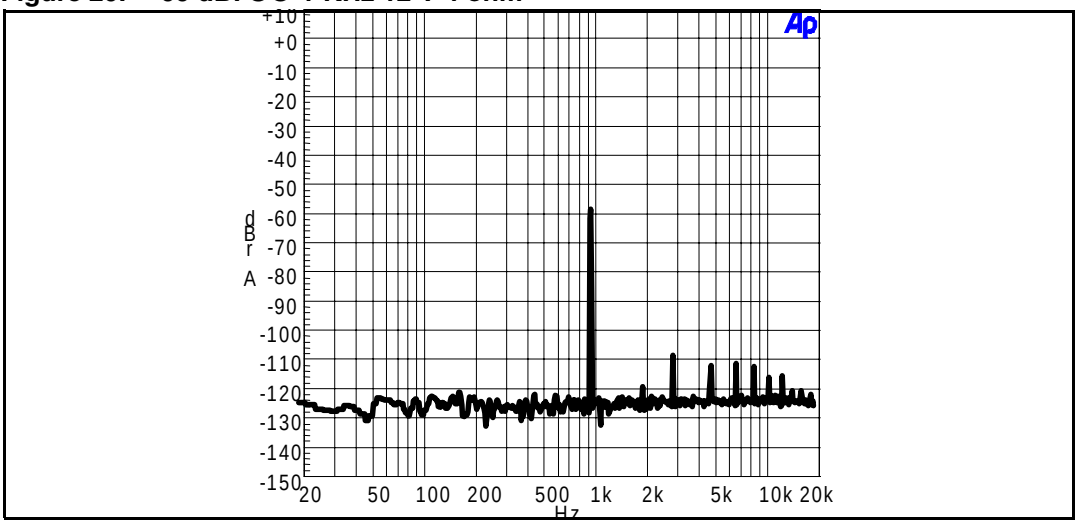


Figure 30. 0 dBFS@ 1 KHz 12 V 6 ohm

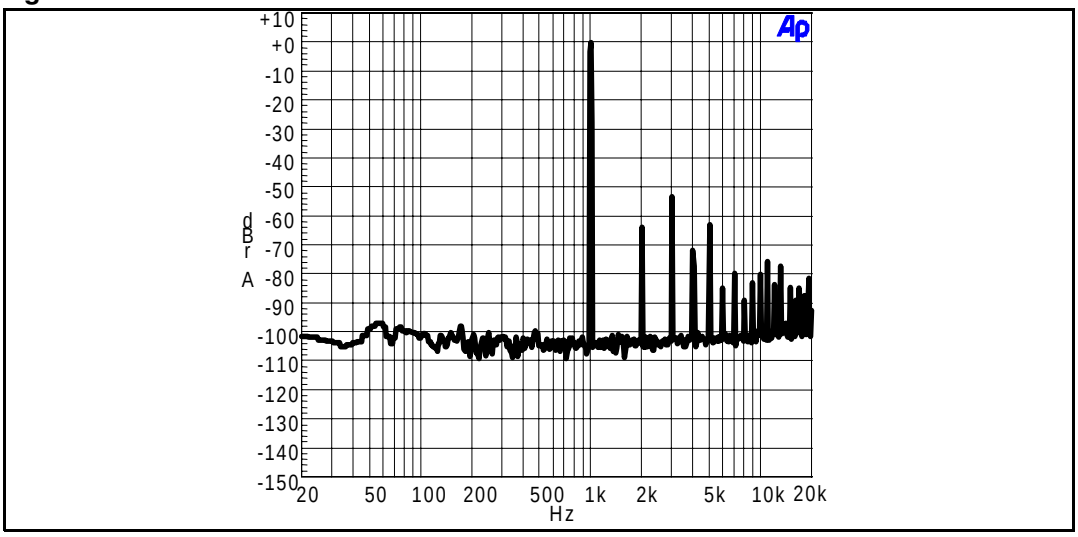


Figure 31. -60 dBFS@ 1 KHz 12 V 6 ohm

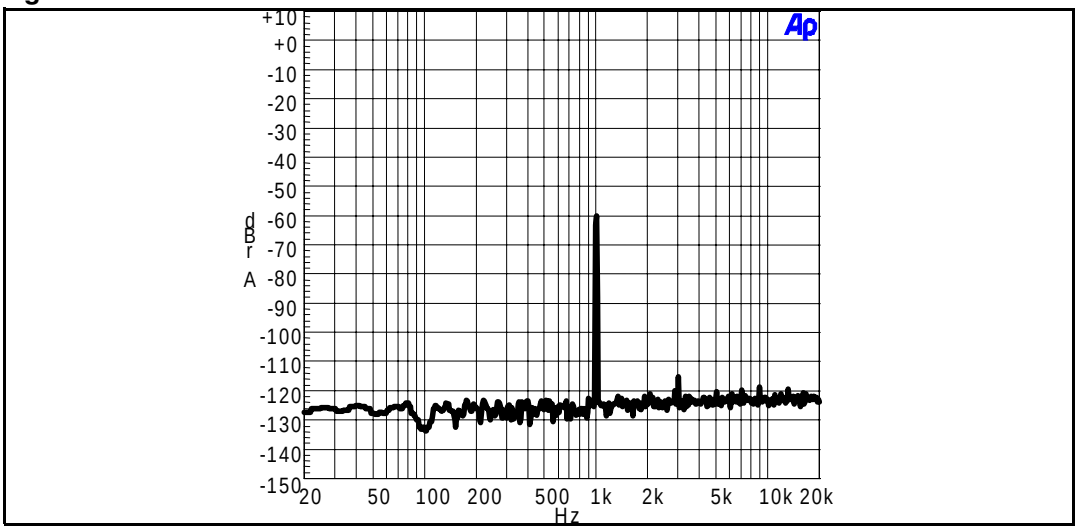


Figure 32. 0 dBFS@ 1 KHz 12 V 8 ohm

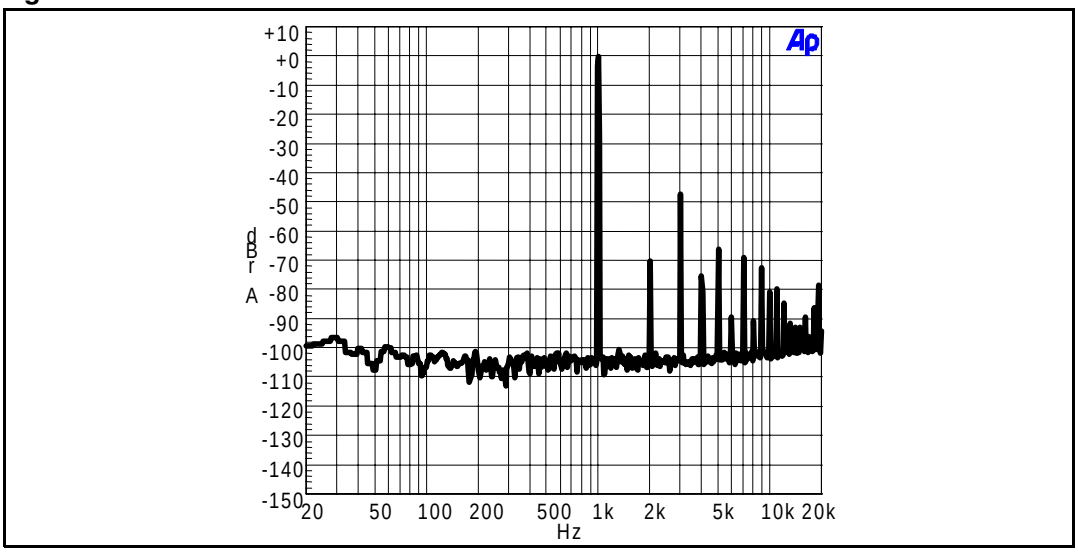


Figure 33. -60 dBFS@ 1 KHz 12 V 8 ohm

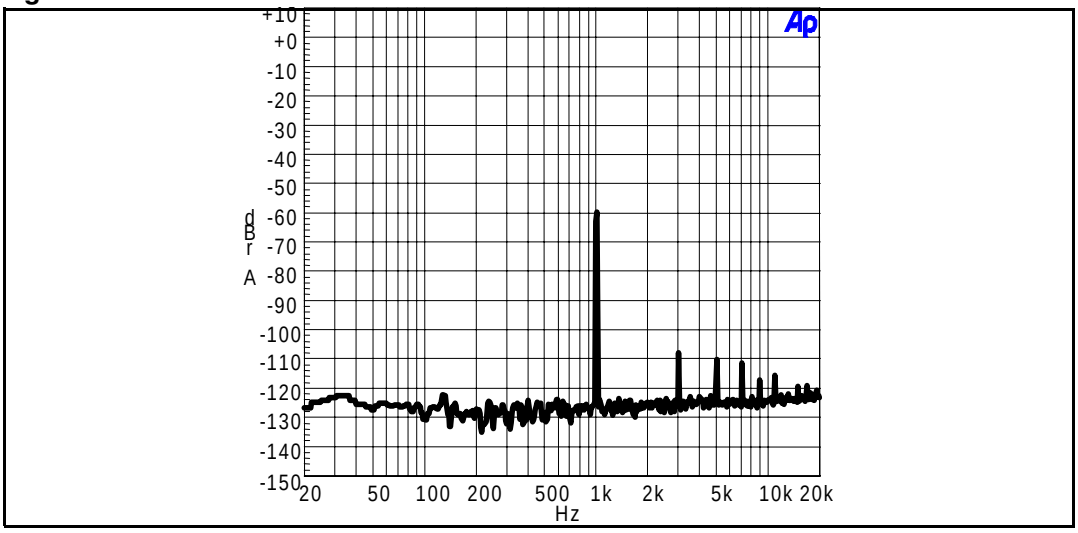


Figure 34. 0 dBFS@ 1 KHz 18 V 4 ohm

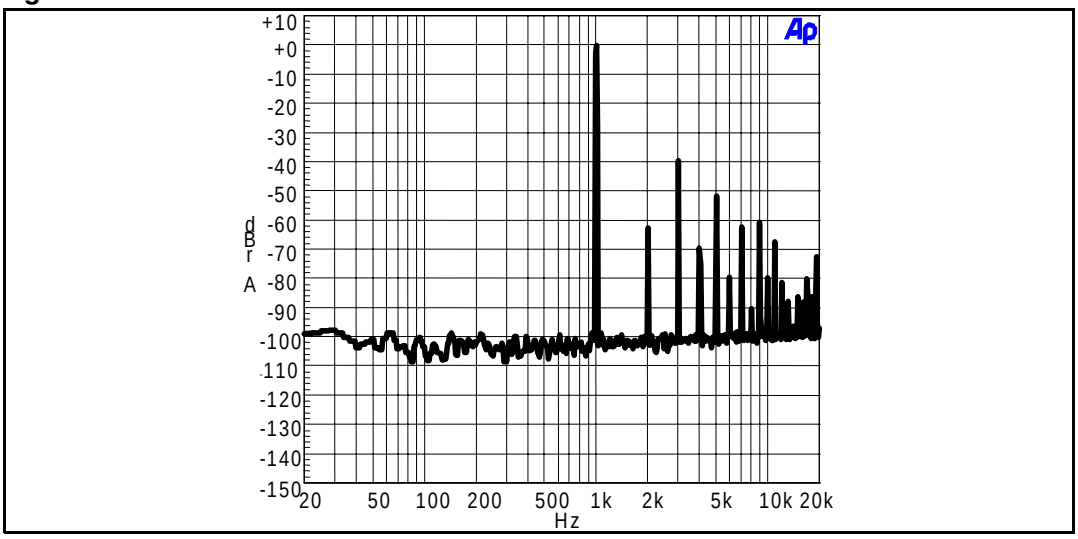


Figure 35. -60 dBFS@ 1 KHz 18 V 4 ohm

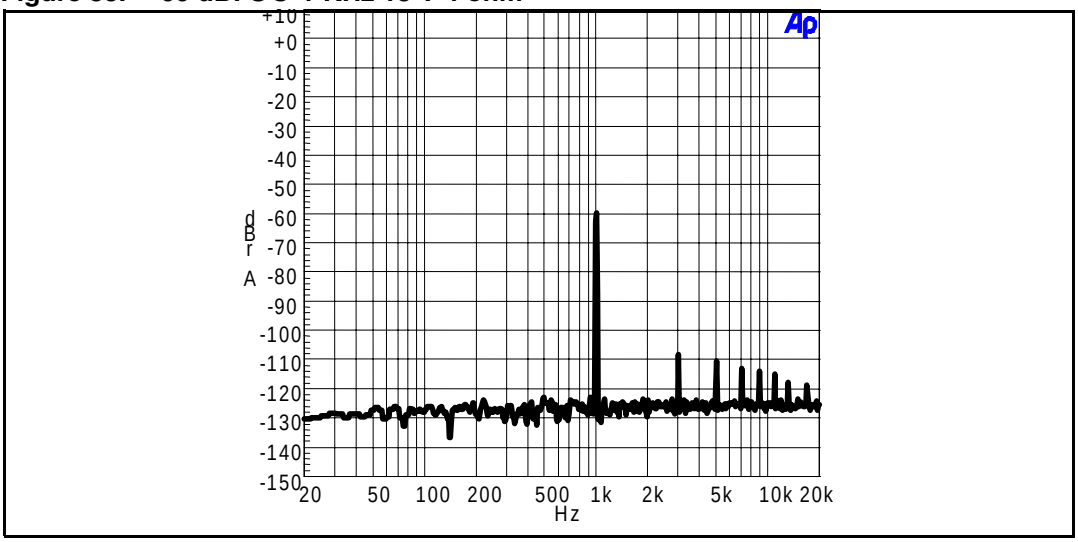


Figure 36. 0 dBFS@ 1 KHz 18 V 6 ohm

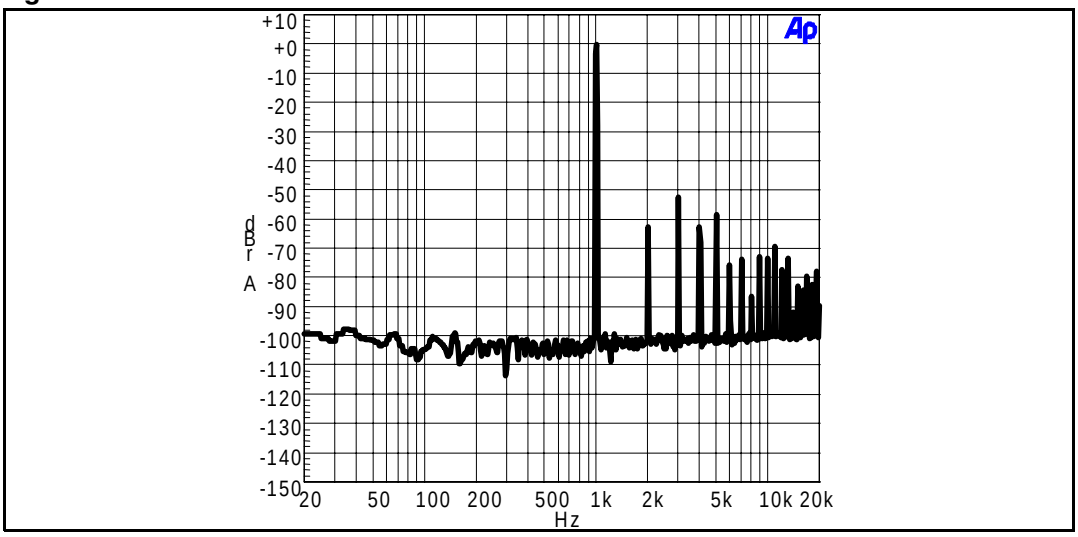


Figure 37. -60 dBFS@ 1 KHz 18 V 6 ohm

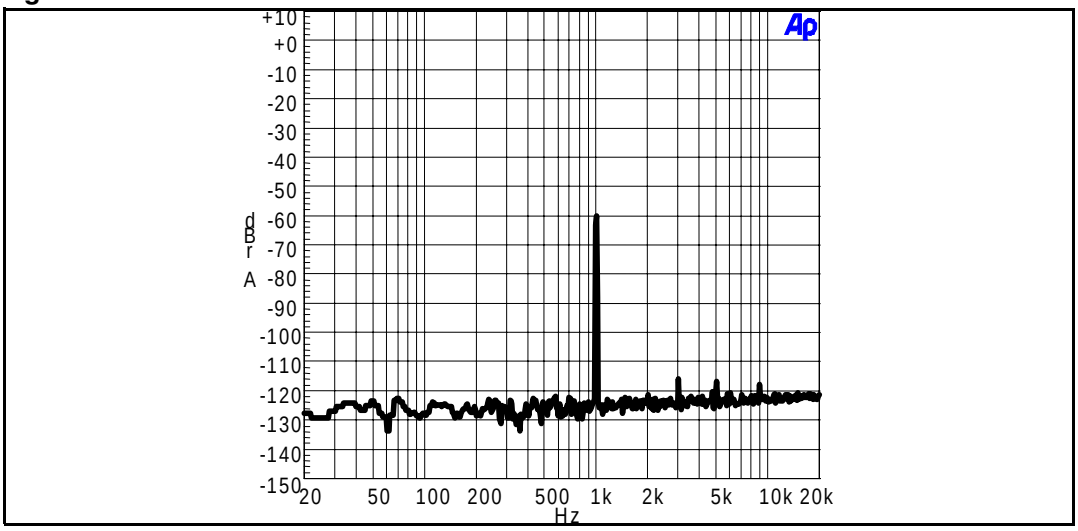


Figure 38. 0 dBFS@ 1 KHz 18 V 8 ohm

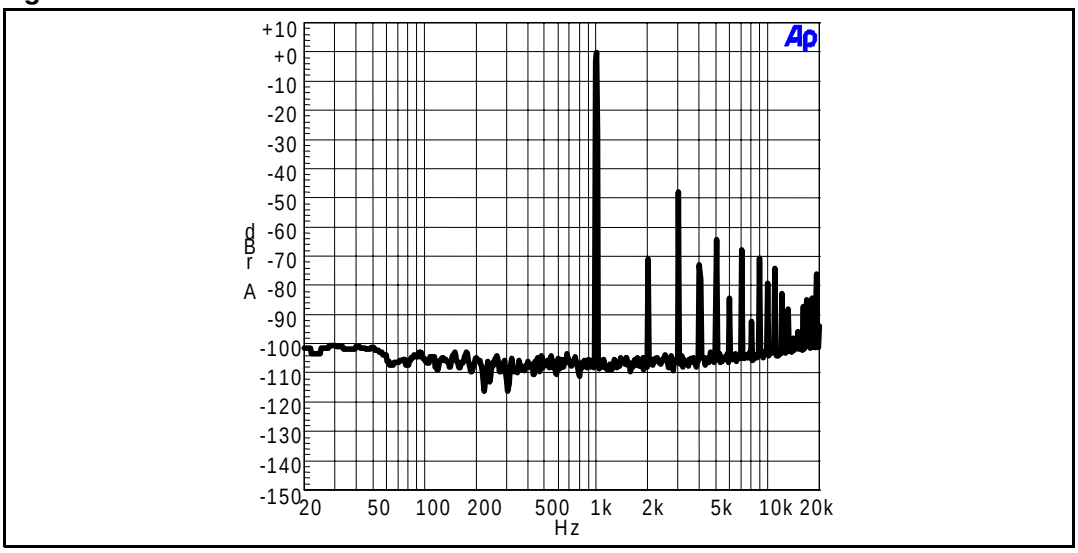
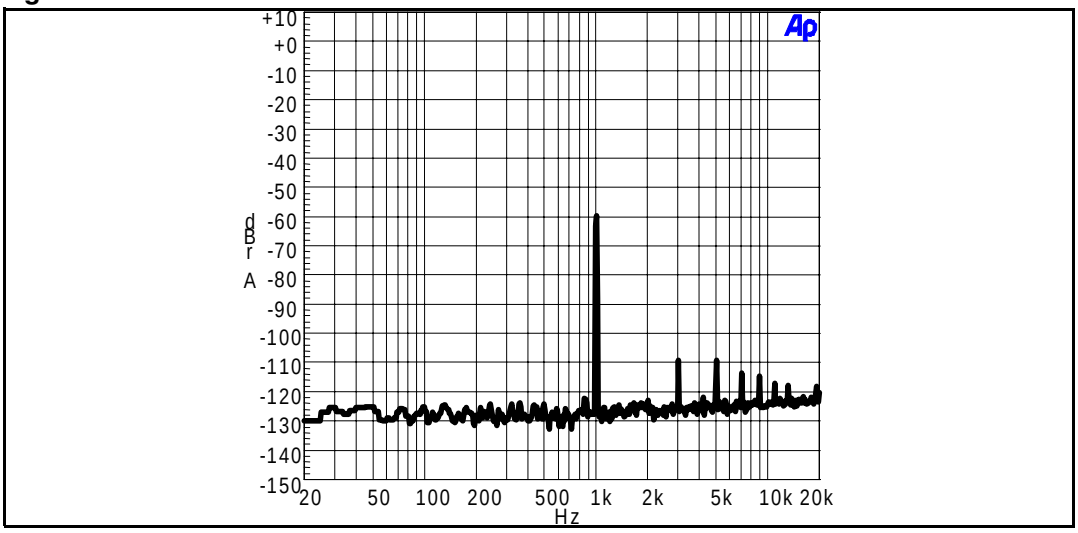


Figure 39. -60 dBFS@ 1 KHz 18 V 8 ohm



2.4 Cross talk

Figure 40. 5 V 4 ohm 1 W @ 1 KHz

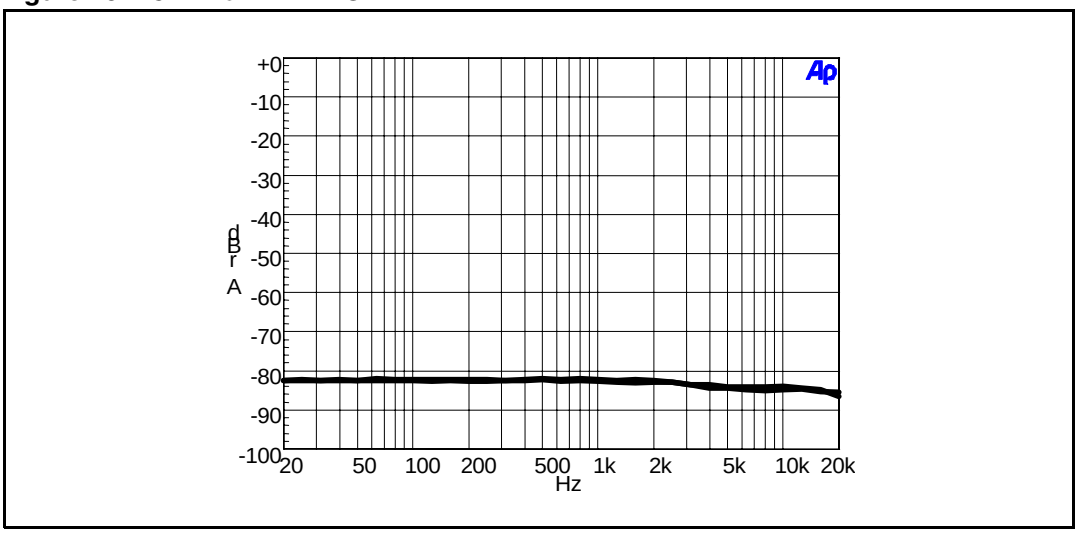


Figure 41. 12 V 4 ohm 1 W @ 1 KHz

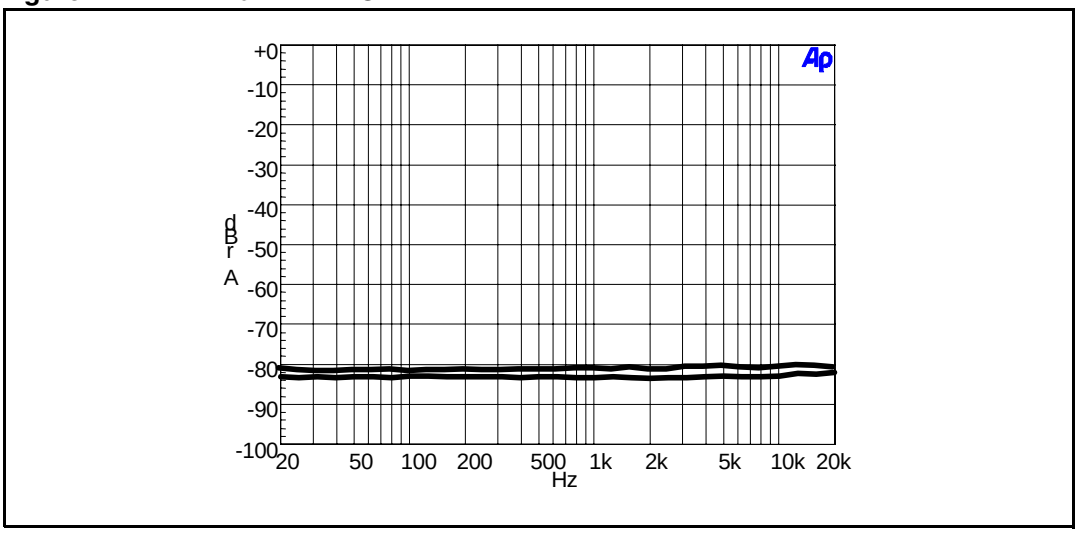


Figure 42. 18 V 4 ohm 1 W @ 1 KHz

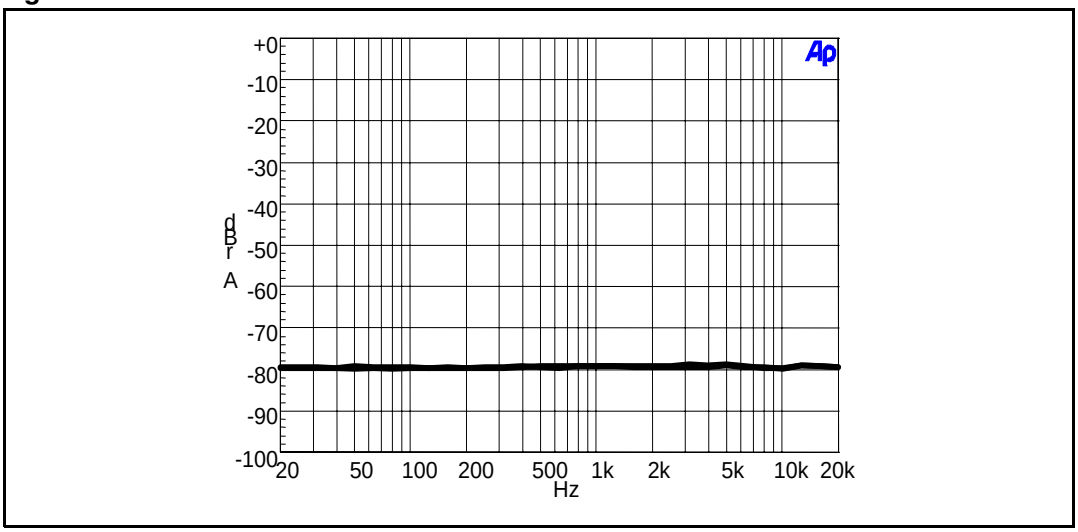


Figure 43. 5 V 6 ohm 1 W @ 1 KHz

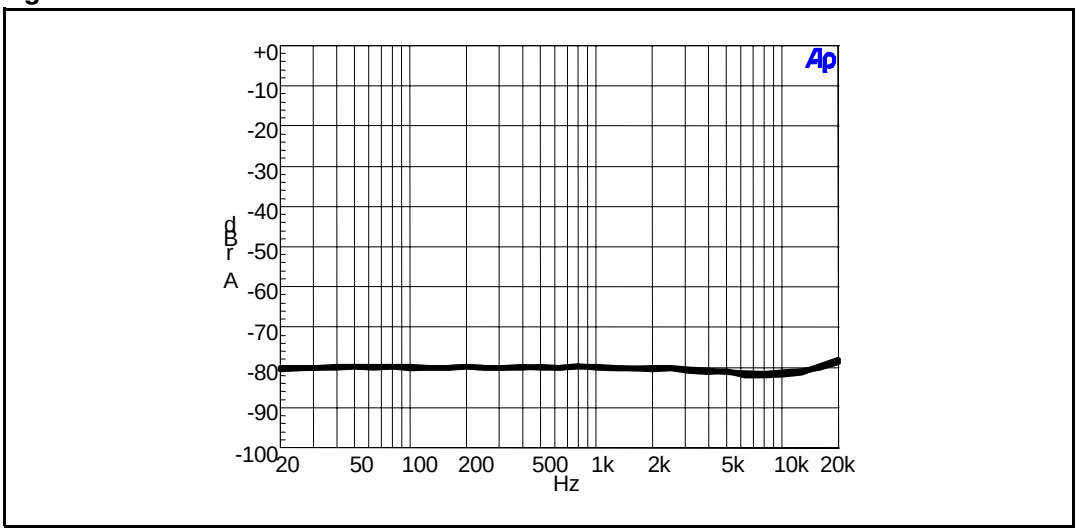


Figure 44. 12 V 6 ohm 1 W @ 1 KHz

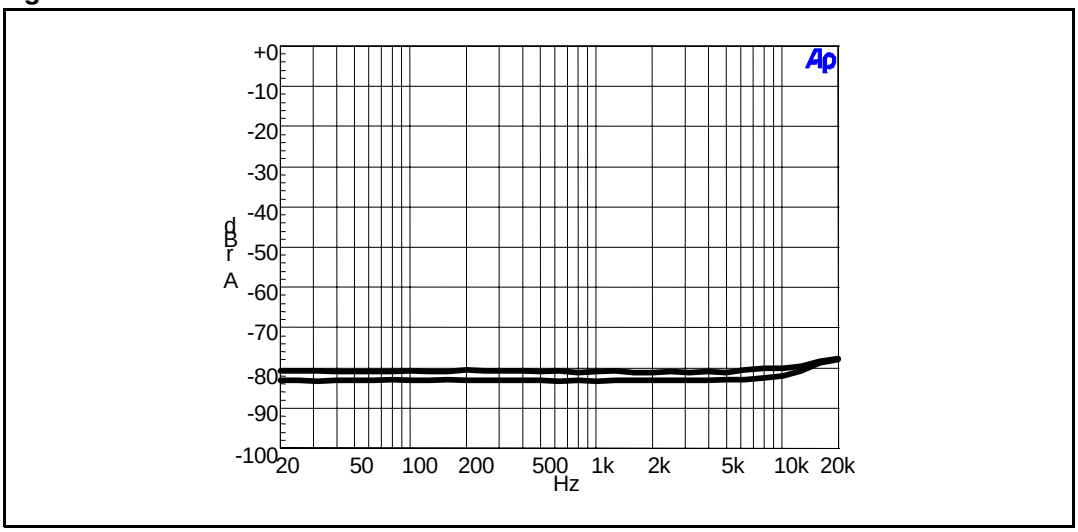


Figure 45. 18 V 6 ohm 1 W @ 1 KHz

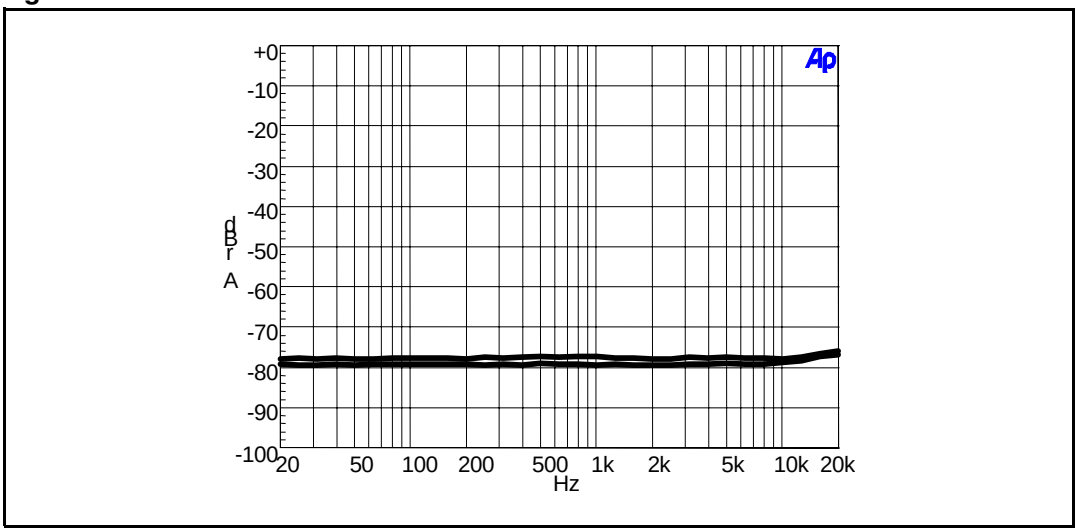


Figure 46. 5 V 8 ohm 1 W @ 1 KHz

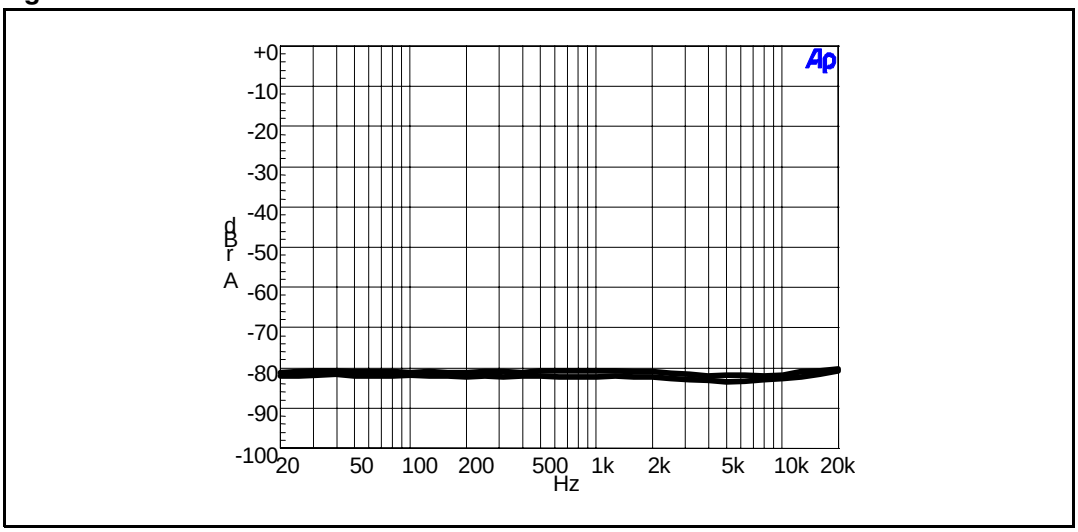


Figure 47. 12 V 8 ohm 1 W @ 1 KHz

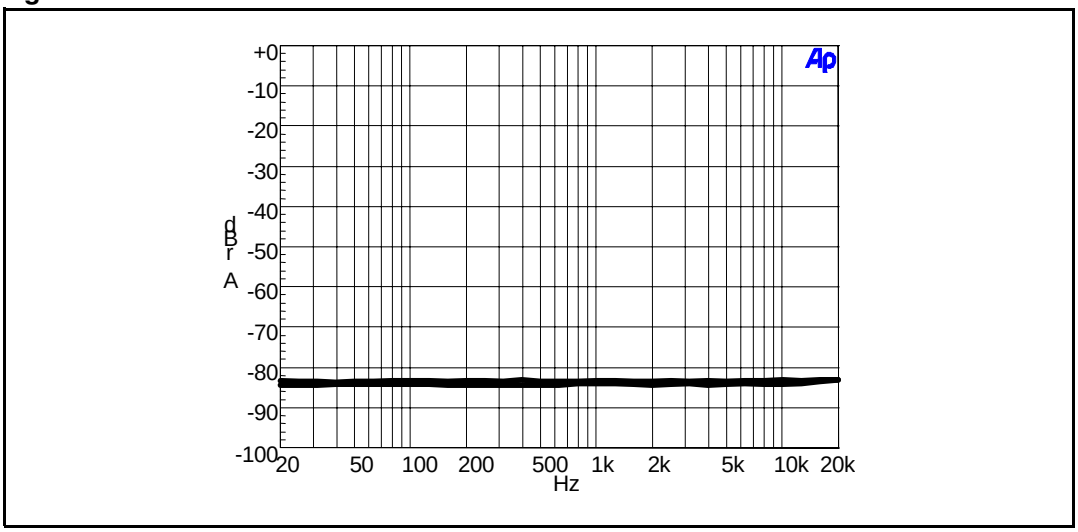
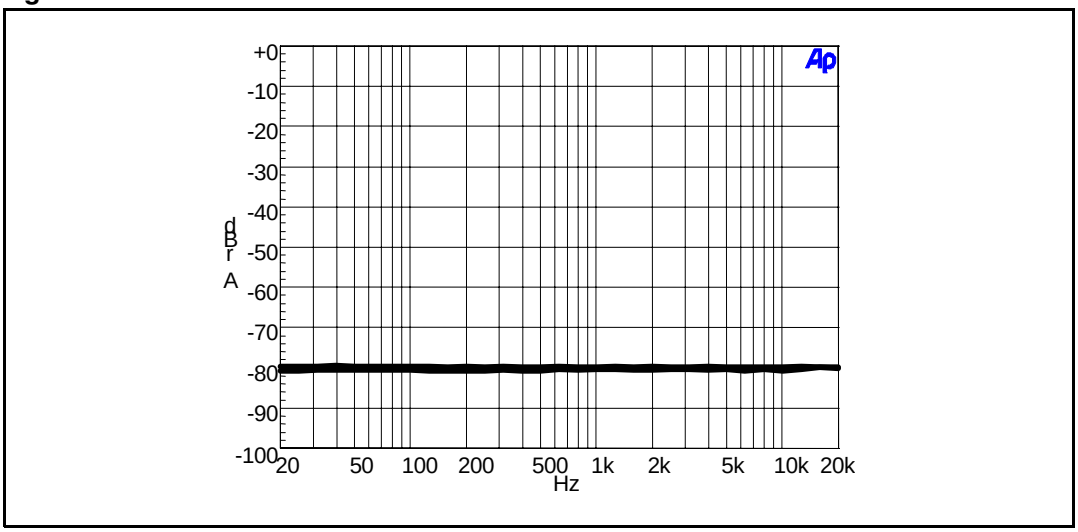


Figure 48. 18 V 8 ohm 1 W @ 1 KHz



3 Design guideline for PCB schematic and layout

3.1 Schematic

3.1.1 Main driver for components selection

- Absolute maximum rate: 20 V.
- Bypass capacitor 100 nF in parallel to 1 µF for each power Vcc branch. Preferable dielectric is X7R.
- Vdd and ground for PLL filter separate of the power supply.
- Coil saturation current compatible with the peak current of the application.

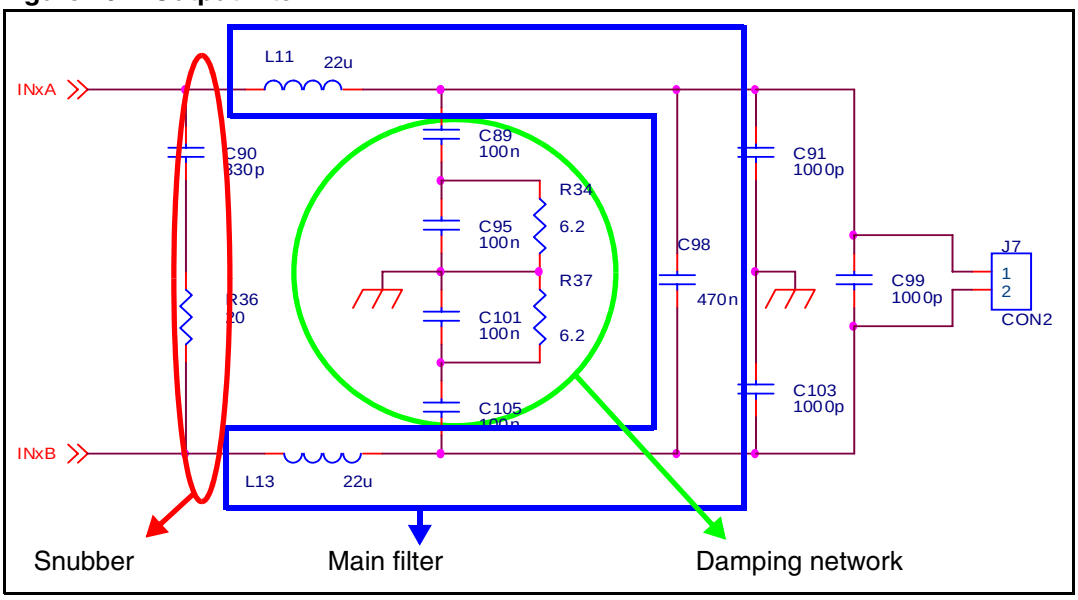
3.2 Decoupling capacitors

There are two different ways to use the decoupling capacitors:

- shared among the channels: the best practise layout route must be used for the board,
- one decoupling system per channel: it is mandatory that the decoupling capacitor must be as close as possible to the IC pins.

3.2.1 Output filter

Figure 49. Output filter



- The key function of a snubber network is to absorb energy from the reactance in the power circuit. The purpose of the snubber RC network is in order to avoid the high pulse energy (such as spikes) in the power circuit which can be dangerous to the system. When using the snubber network, the energy is be transferred to and from the snubber network, ensuring the system can work safely.

- The purpose of the main filter is to remove frequency higher than audible range of 20 KHz. The main filter uses the Butterworth formula to define the cut off frequency, which must be higher than 20 KHz, otherwise the frequency response is affected.
- The purpose of the damping network is to avoid high frequency oscillation on the output circuit. After using the damping network the THD can be improved, and can also avoid the inductive copper on the PCB route when the system is working in high frequency with PWM or PCM.

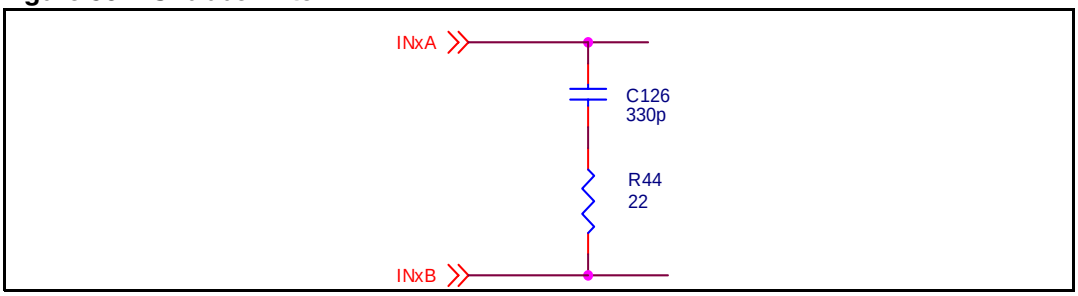
Snubber filter

The snubber circuit must be optimized for the application. Starting values are 330 pF in series to 22 ohm. The power can be defined by the following formula which considers the power supply, frequency and capacitor value:

P=C*f*(2*V)^2

This power is dissipated in series resistance.

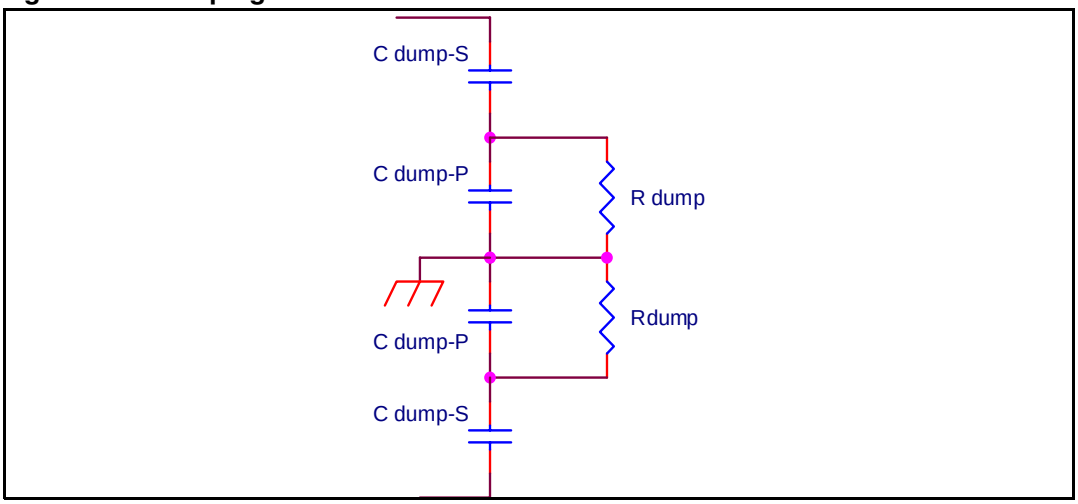
Figure 50. Snubber filter



Damping network

The C-R-C is a damping network. It is mainly intended for high inductive loads.

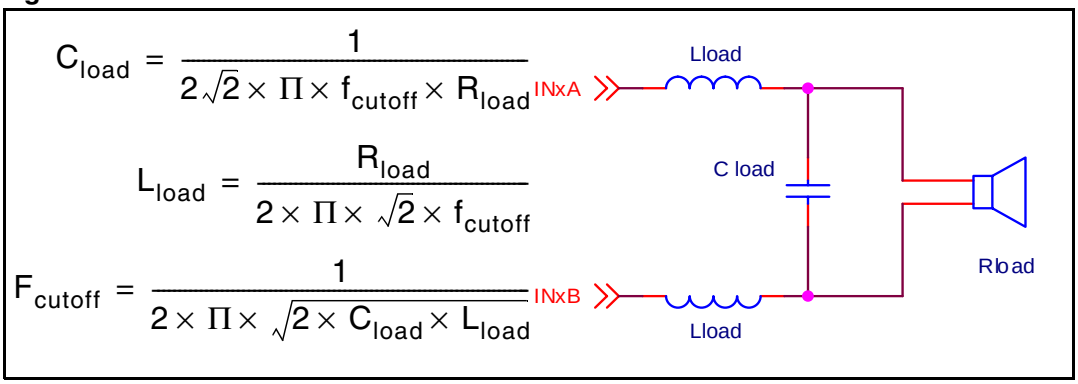
Figure 51. Damping filter



Main filter

The main filter is an L and C based Butterworth filter. The cut-off frequency must be chosen between the upper limit of the audio band (20 KHz) and the carrier frequency (384 KHz).

Figure 52. Main filter

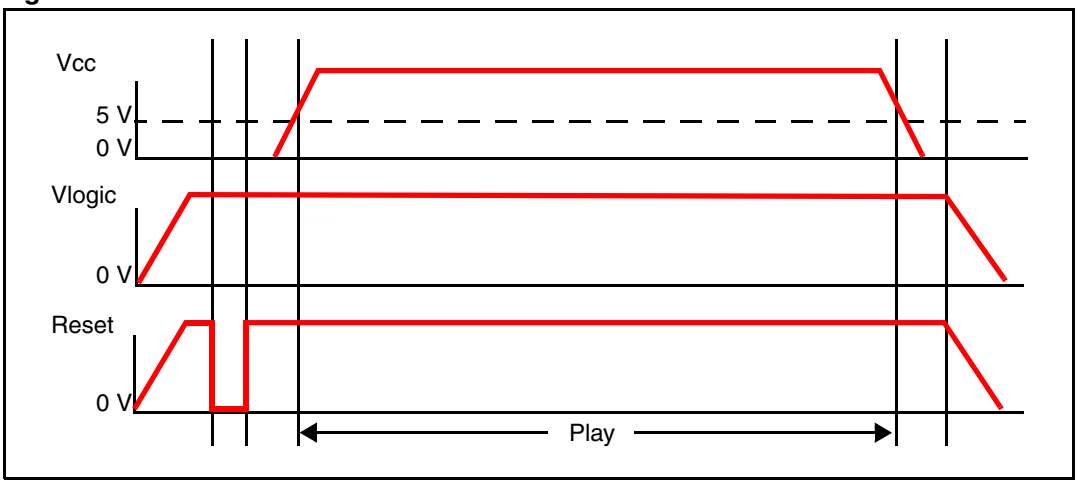

$C_{load} = \frac{1}{2\sqrt{2} \times \Pi \times f_{cutoff} \times R_{load}}$
$L_{load} = \frac{R_{load}}{2 \times \Pi \times \sqrt{2} \times f_{cutoff}}$
$F_{cutoff} = \frac{1}{2 \times \Pi \times \sqrt{2 \times C_{load} \times L_{load}}}$
INxA
INxB
Lload
C load
Rload
Lload

Recommended values

Rload	8 ohm	4 ohm
Lload	22 µH	10 µH
Cload	470 nF	1 µH
C dump-S	100 nF	220 nF
C dump-P	220 nF	220 nF
R dump	6.2	2.7

Recommended power up and power down sequence

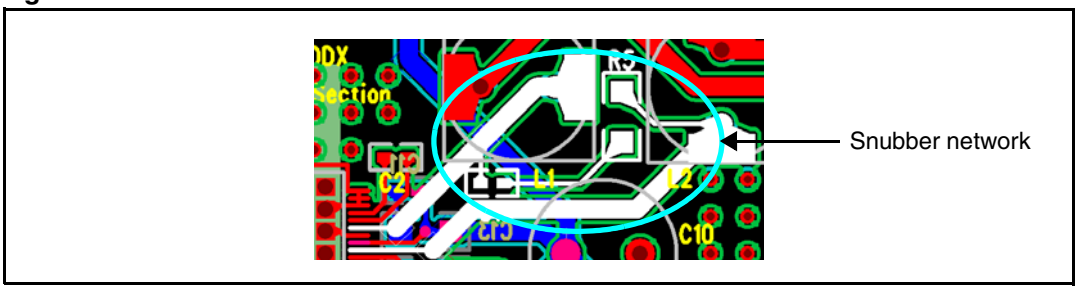
Figure 53. Main filter



3.3 Layout

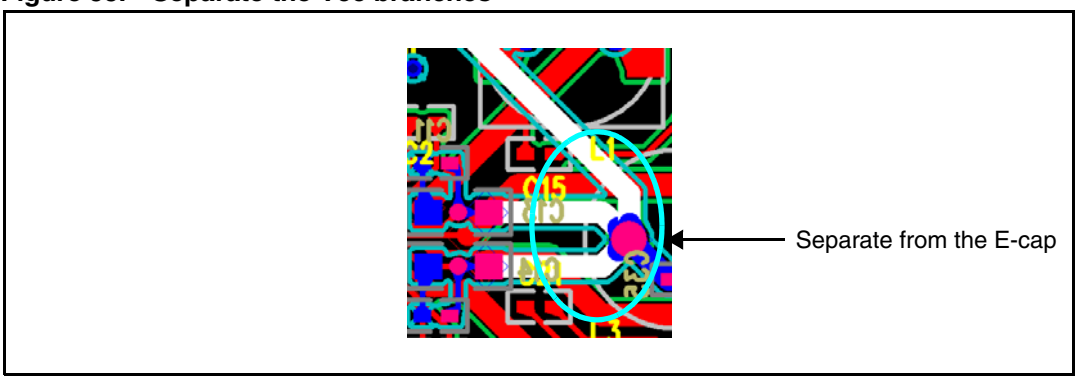
1. Solder snubber network as close as possible to the IC related pin.

Figure 54. Snubber network



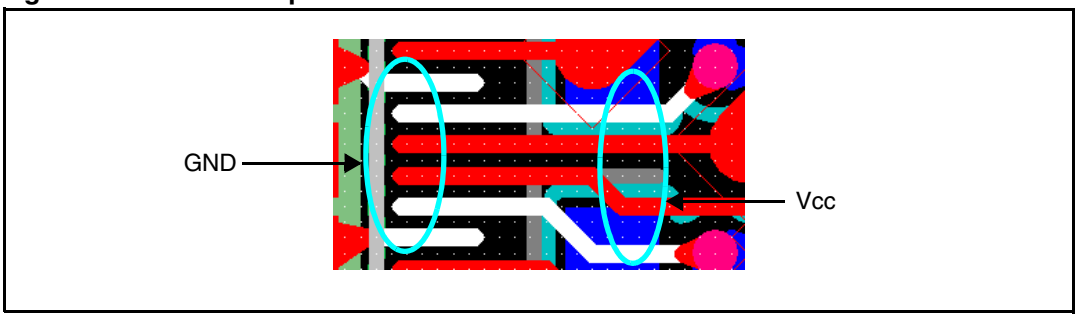
2. Use electrolytic capacitor first to separate the Vcc branches.

Figure 55. Separate the Vcc branches



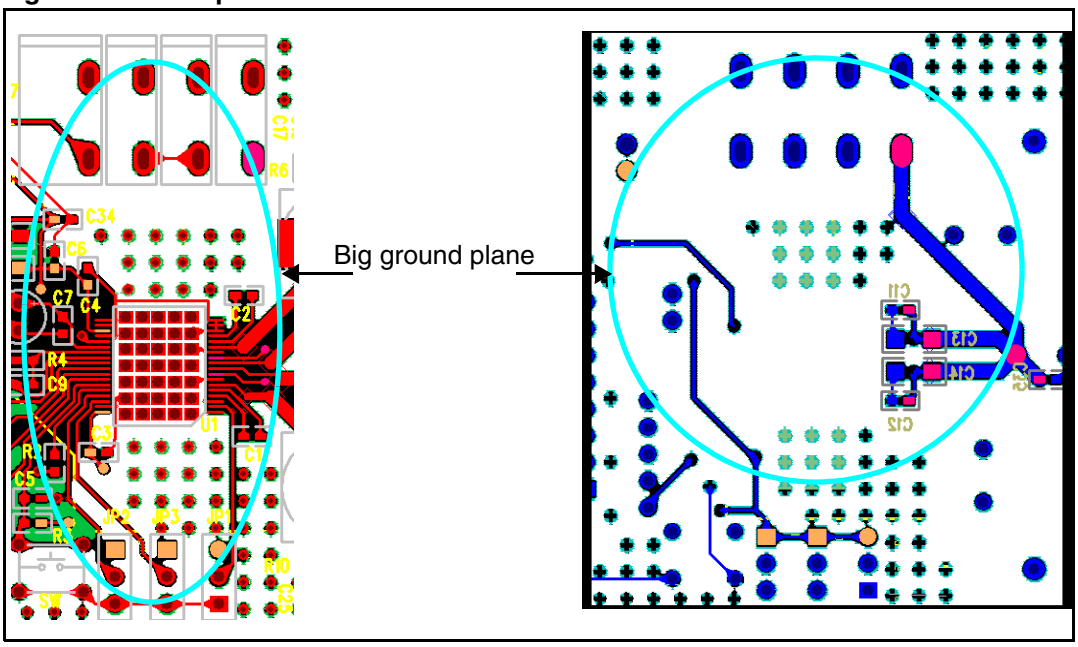
3. Minimize the path between Vcc pins and ground pin in order to avoid inductive paths.

Figure 56. Minimized paths between Vcc and GND



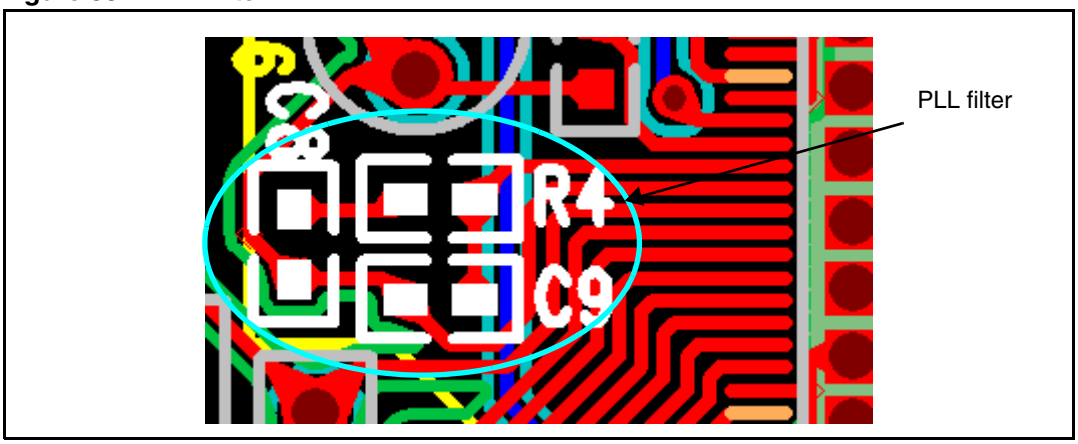
4. To dissipate the thermal with a ground plane.

Figure 57. Dissipate thermal



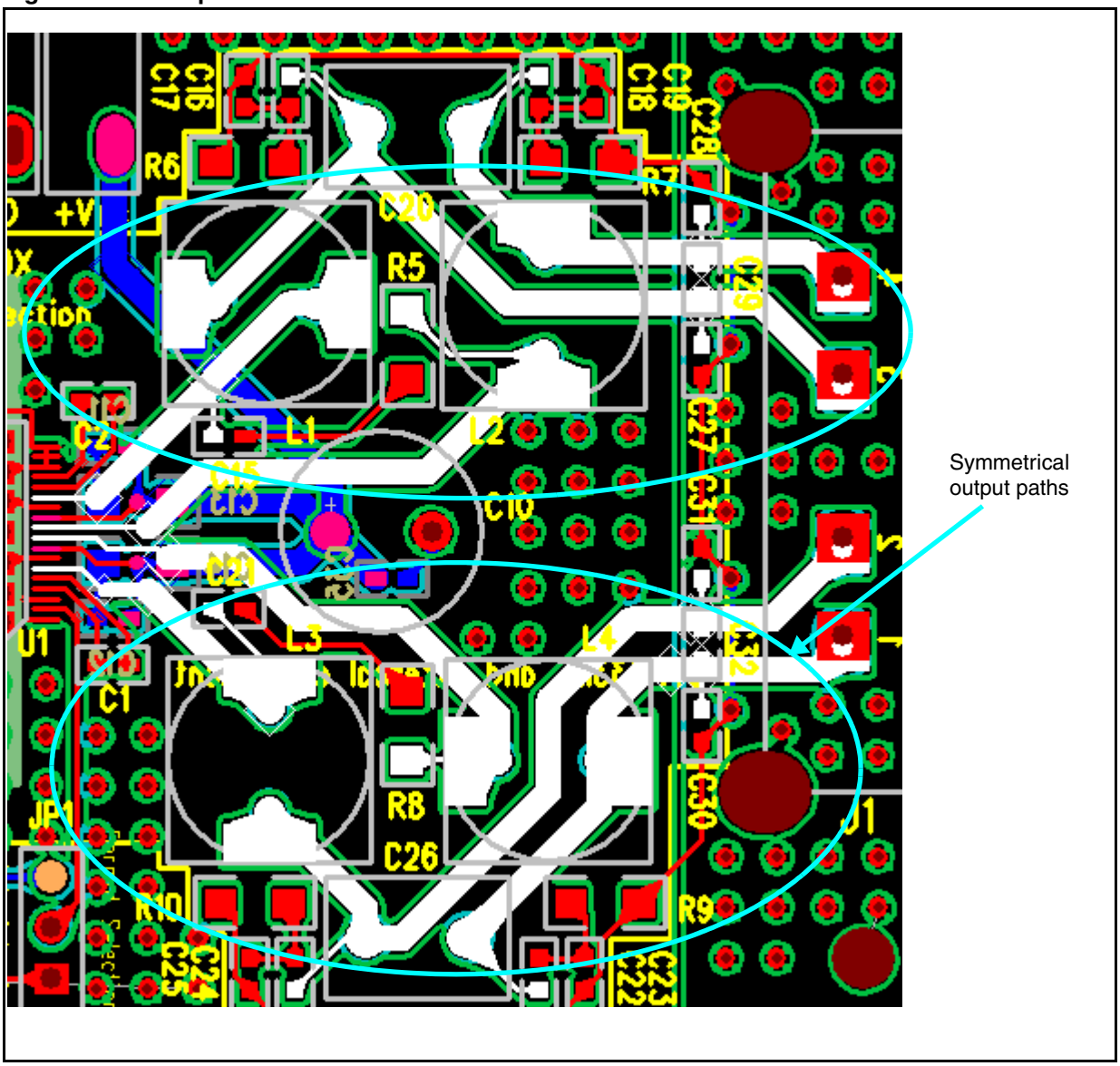
5. Solder PLL filter as close as possible to the FILT pin.

Figure 58. PLL filter



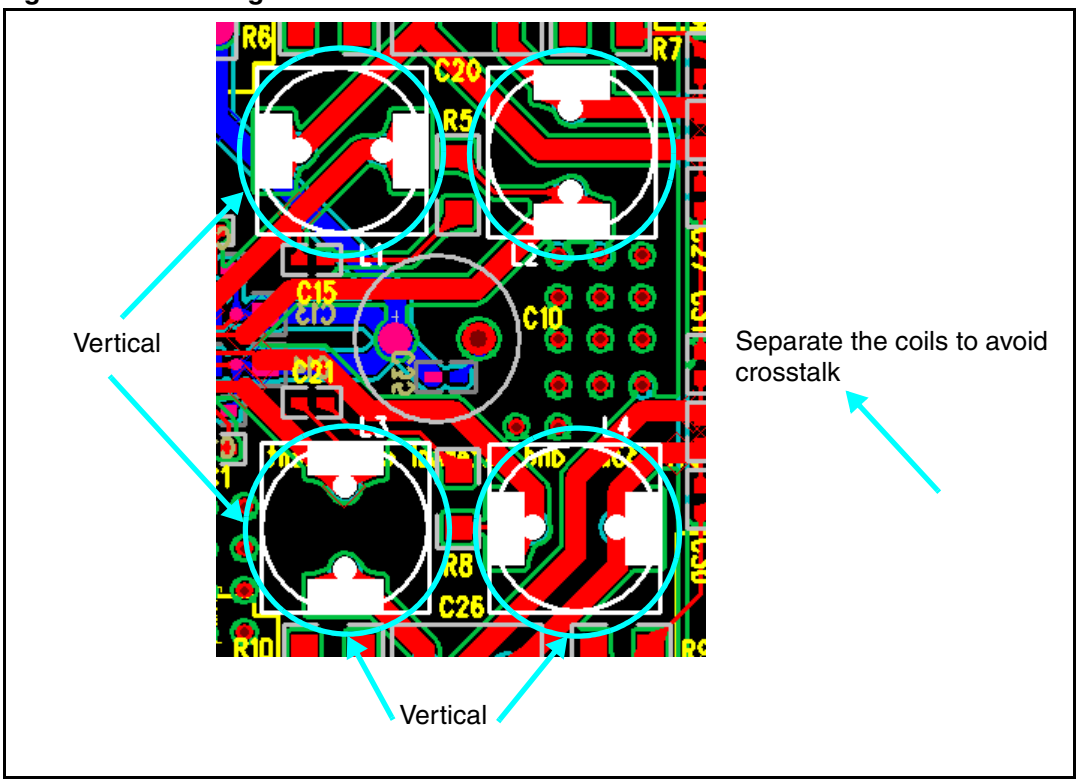
6. For differential application create symmetrical paths for the output stage.

Figure 59. Dissipate thermal



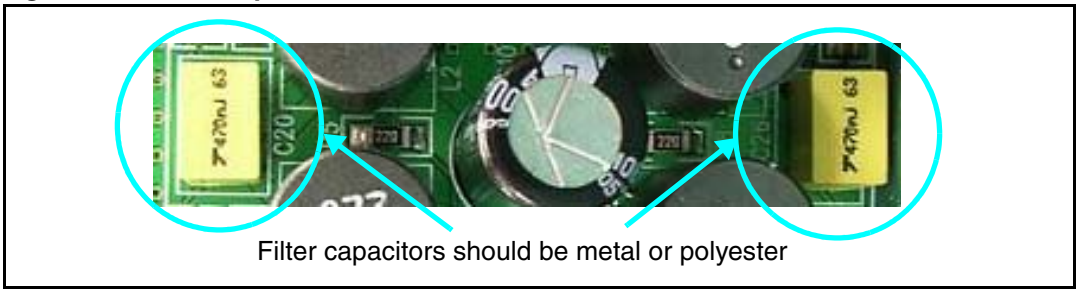
7. Separate the coil and the neighboring coil are vertical to avoid crosstalk.

Figure 60. Avoiding crosstalk



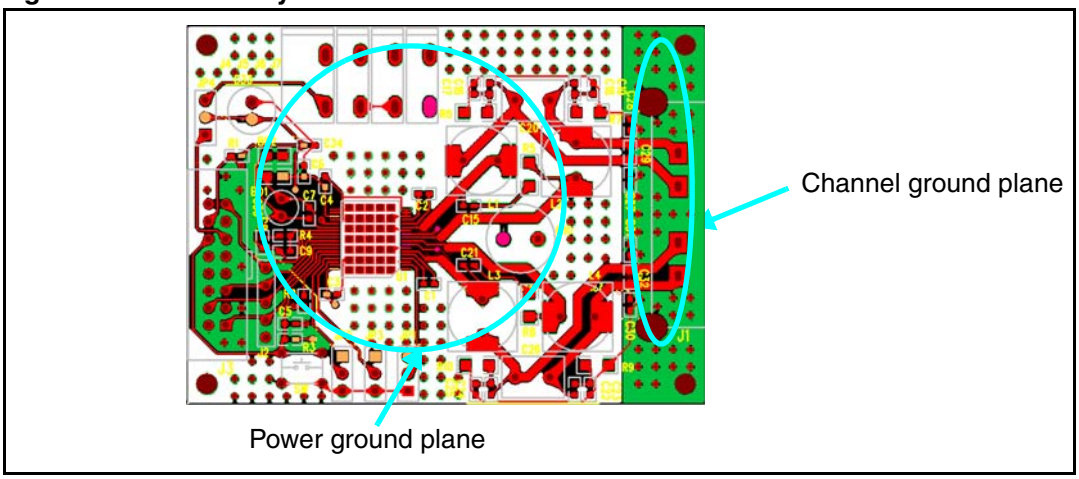
8. It is better to use a polyester filter capacitor.

Figure 61. Filter capacitor



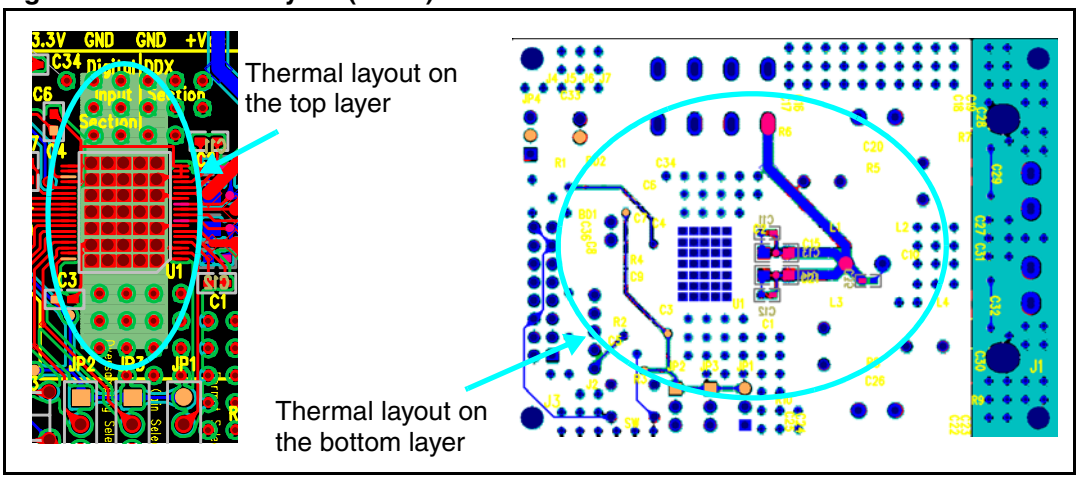
9. Consider ground layout. To avoid interference between ground power and small signal ground, it is necessary to divide the grounding as shown in *Figure 62*.

Figure 62. Ground layout



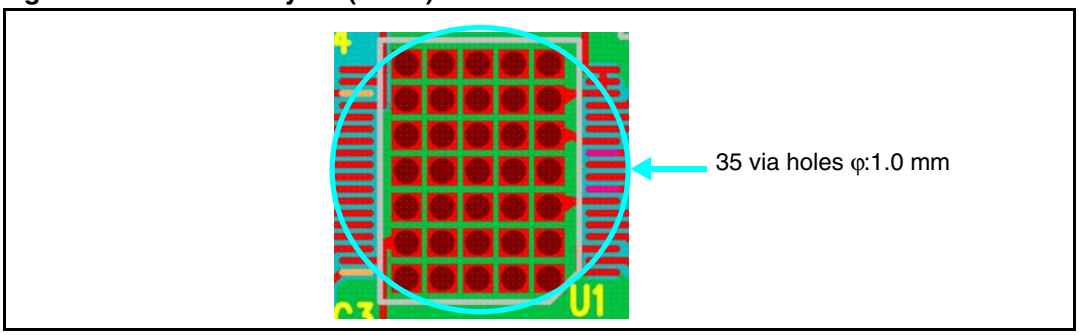
10. Thermal layout with large ground (1 of 2 for top and bottom layers).

Figure 63. Thermal layout (1 of 2)



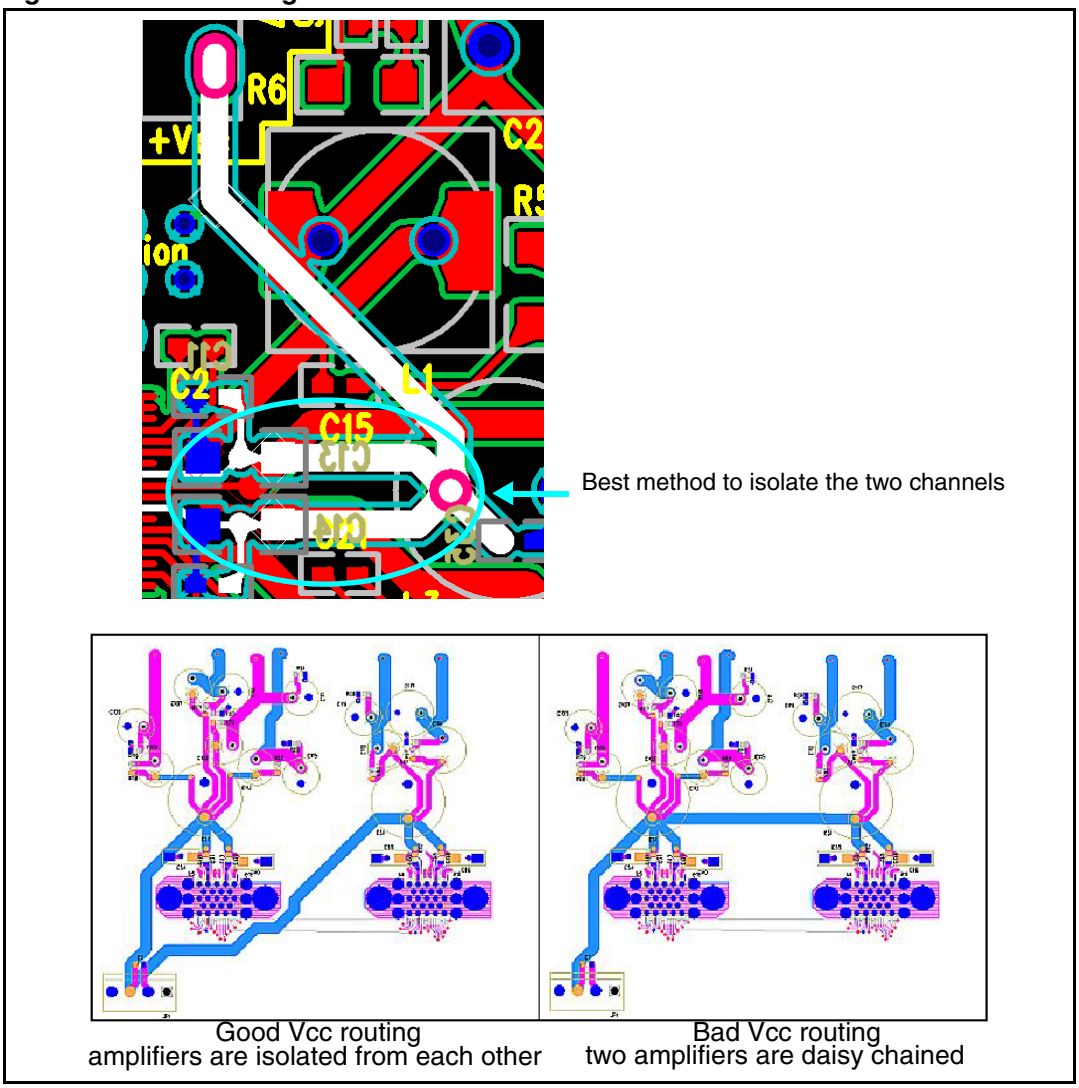
11. Thermal layout with big ground (2 of 2 for thermal and soldering holes).
The thermal resistance junction at the bottom of the STA333ML to the ambient obtainable with a ground copper area of 4 x 4 cm and with 35 via holes (see *Figure 64*).

Figure 64. Thermal layout (2 of 2)



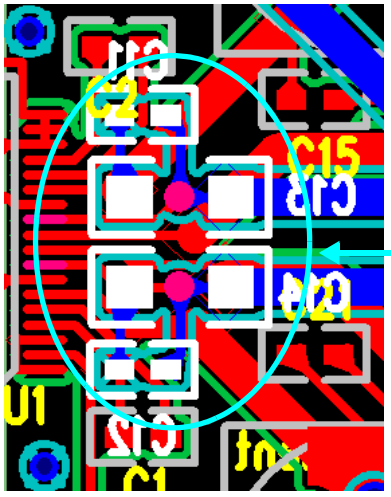
12. VCC routing.
The best route for the Vcc supply is one which avoids interference between different signals (for example, part A is idle whilst part B is working at full load).

Figure 65. Vcc routing



13. Vcc filter for high frequency.
The PWM system works with a fast switch (frequency of 340 KHz approximately) which means the copper wire works as a coil. In order to avoid this, a ceramic capacitor should be used to balance resistance. It is a mandatory requirement that ceramic capacitors are placed as close as possible to the related pins. The distance between the capacitor and their respective pins should be less then 5 mm in order to minimize inductive coil effect generated by the copper wire.

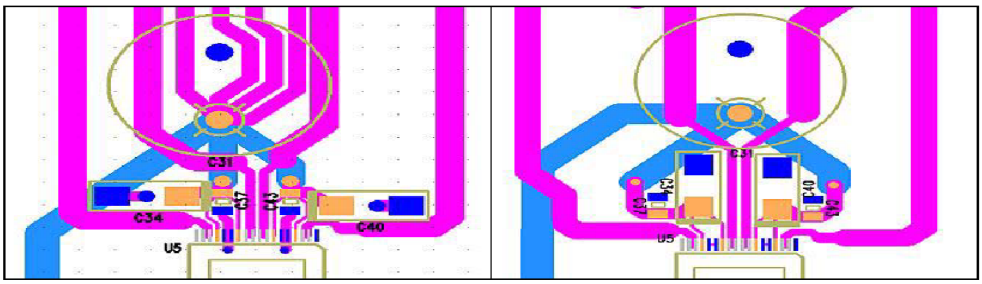
Figure 66. Vcc filter



Vcc capacitor filter as close to the related pins as possible. The ceramic capacitors on the bottom of the PCB close to the IC due to SMD mounting limitations.

14. Decoupling capacitors.
Solder decoupling capacitors as close as possible to their respective IC pin. This reduces the inductive coil effect.

Figure 67. Decoupling capacitors



Good amplifier bypassing capacitors are properly placed

Bad amplifier bypassing, capacitors are out of order and ground connection is indirect

15. Snubber filters for high frequency spike protection on the PWM.

Figure 68. Snubber filter placement

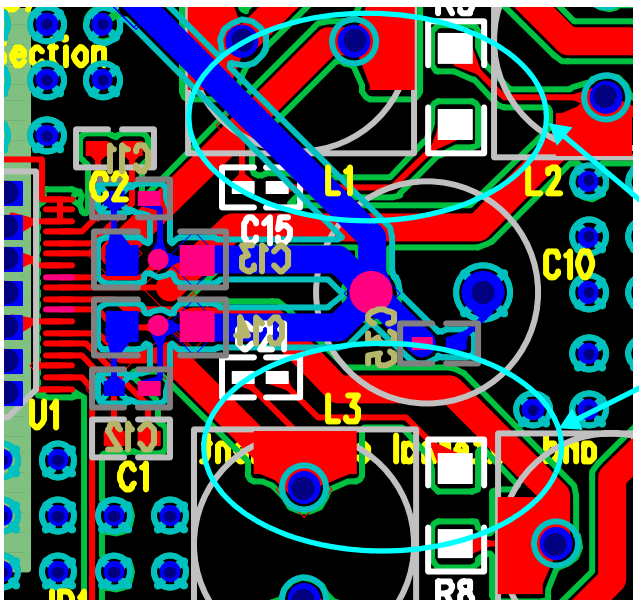
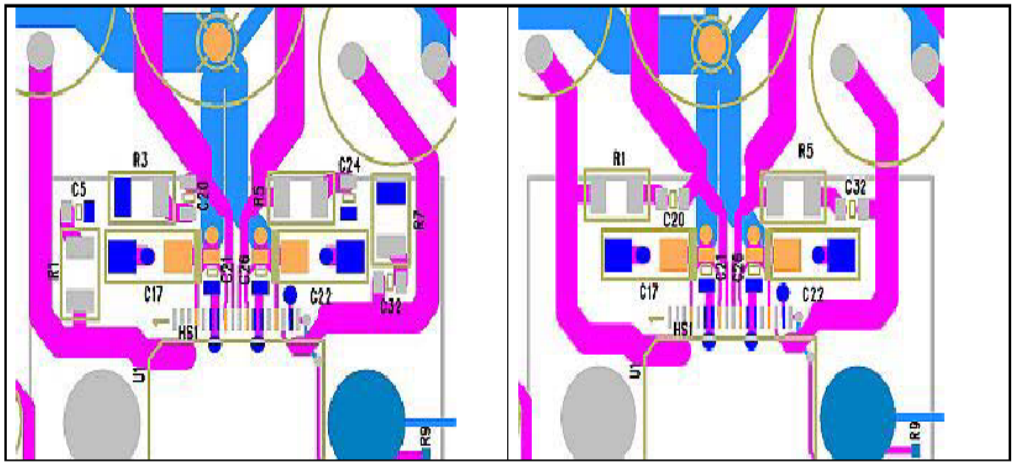


Figure 69. Examples of snubber filter placement

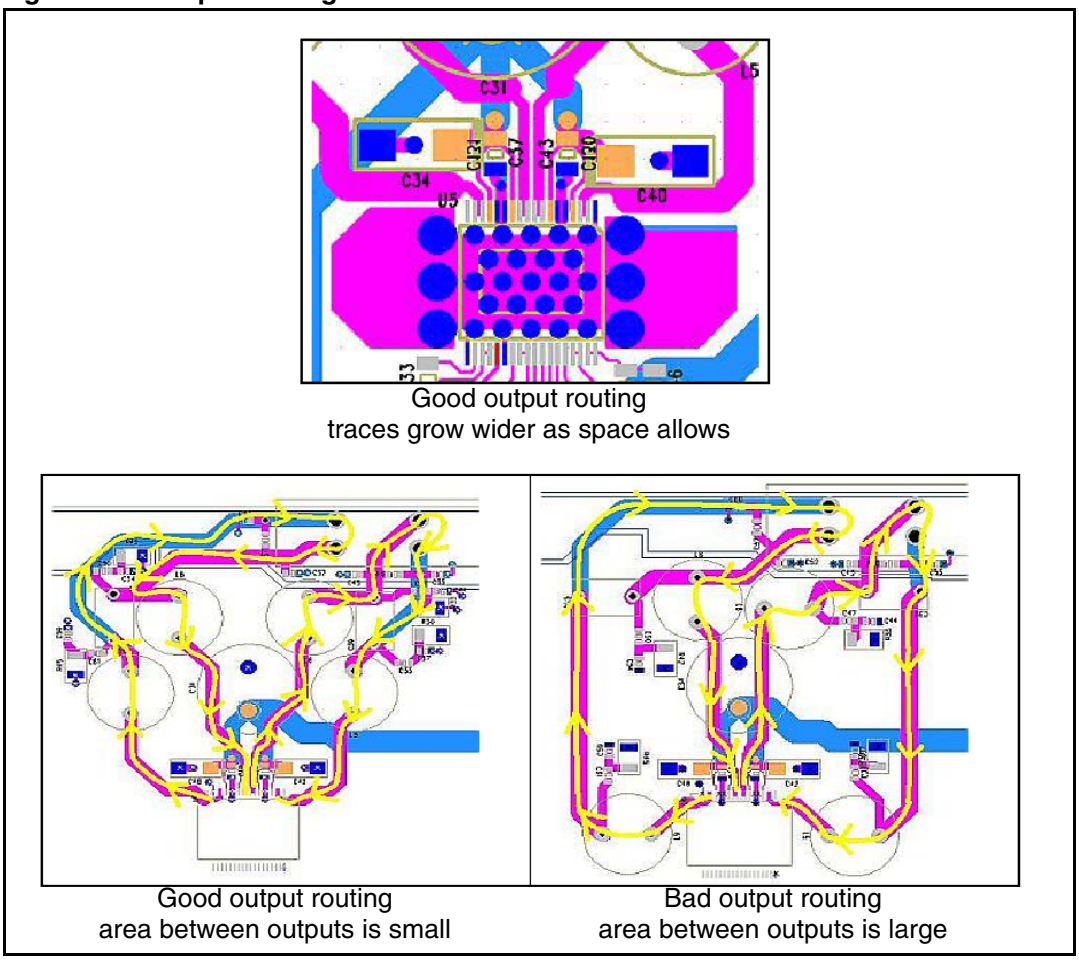


Good common mode snubber placement Good differential snubber placement

Caution: A spike can occur if there > 3 mm distance between the snubber network and the pins. This can cause damage to the IC. Therefore the distance must be kept below 3 mm.

16. Output routing

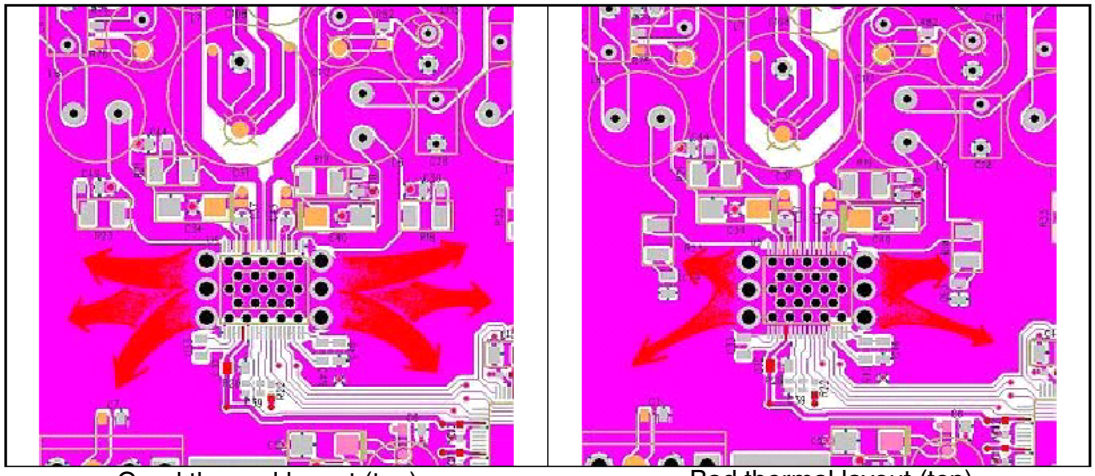
Figure 70. Output routing



17. Thermal layout

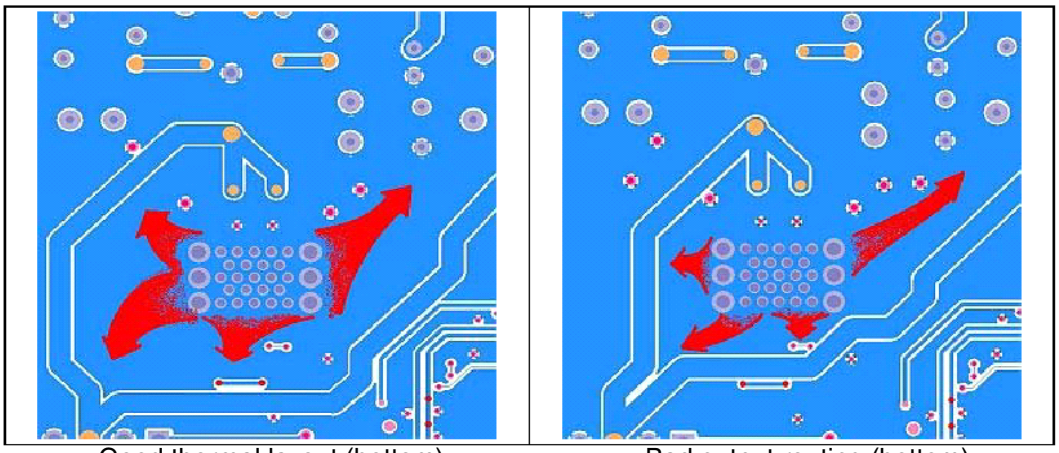
Note: The thermal pad must be connected to ground in order to properly set the IC references. It is necessary to allow the heat to flow freely to all sides of the board including top and bottom. For optimum heat dissipation it is recommended that the PCB has some solder via holes.

Figure 71. Output routing



Good thermal layout (top)
heat can flow freely to the sides

Bad thermal layout (top)
heat flow cut off by the snubbers



Good thermal layout (bottom)
plenty of copper area

Bad output routing (bottom)
little copper area on 3 sides

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
06-Dec-2006	1	Initial release.

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